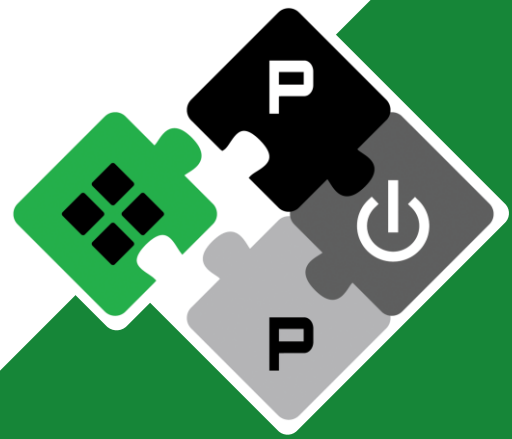
ETH zürich ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA

Iguana: An End-to-End Open-Source Linux-capable RISC-V SoC in 130nm CMOS

Integrated Systems Laboratory (ETH Zürich)

Thomas Benz tbenz@iis.ee.ethz.ch
Paul Scheffler paulsc@iis.ee.ethz.ch
Jannis Schönleber janniss@iis.ee.ethz.ch



PULP Platform
Open Source Hardware, the way it should be!

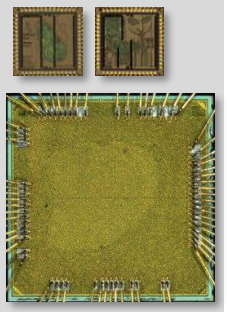
@pulp_platform
pulp-platform.org
youtube.com/pulp_platform

Parallel Ultra Low Power (PULP) Platform

- **Research on open-source energy-efficient computing architectures**

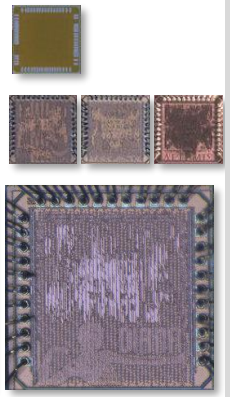
We Have Designed And Tested More Than 50 PULP ICs

2013 (3)



PULPv1
STM 28FDSOI
Multi-core processor

2014 (5)

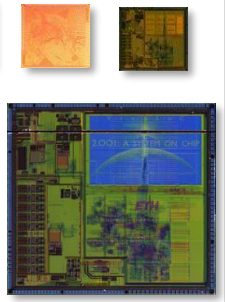


Diana
UMC 65
4-core system with approximate FPUs

2015 (10)

Fulmine
UMC 65
4-core system with ML and Crypto accelerators

2016 (3)

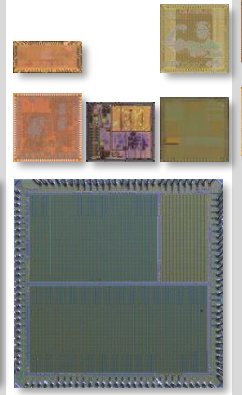


VivoSoC 2.001
SMIC 130
Mixed signal system for biosignal acquisiton

2017 (2)

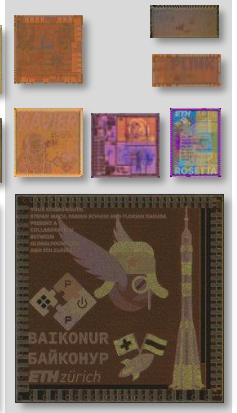
Mr. Wolf
TSMC 40
8+1 core IoT processor

2018 (6)



Poseidon
GF 22FDX
64bit RISC-V core, 32bit Microcontroller system, ML ...rator

2019 (7)



Baikonur
GF 22FDX
Dual 64bit RISC-V core, 3x 8core snitch clusters, Body biasing test vehicle

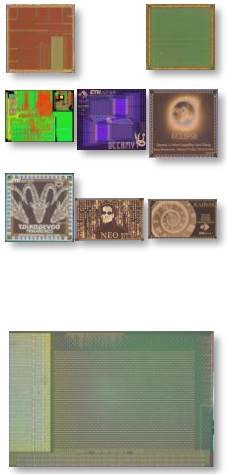
2020 (3)

Dustin
TSMC 65
IoT processor with 16 cores and QNN enhancements

2021 (7)

Kraken
GF 22FDX
IoT processor with Spiking Neural and Ternary Inference Engines

2022 (9)



Occamy
GF 12LPP
ML accelerator with 216 + 1 cores and HBM interface

Check http://asic.ethz.ch for all our chips

Education At IIS And Open EDA FLow

- **At IIS: VLSI lecture series: VLSI I – IV**
  - Bachelor & Master-level
  - RTL design – ASIC design – Custom standard cell design – ASIC testing

http://asic.ethz.ch

- **5-10 student chips every year**
  - Starting from the **3rd year (Bachelor),** teams of 2-3 students, **RTL to tapeout**
  - **7** undergrad students helped with Iguana

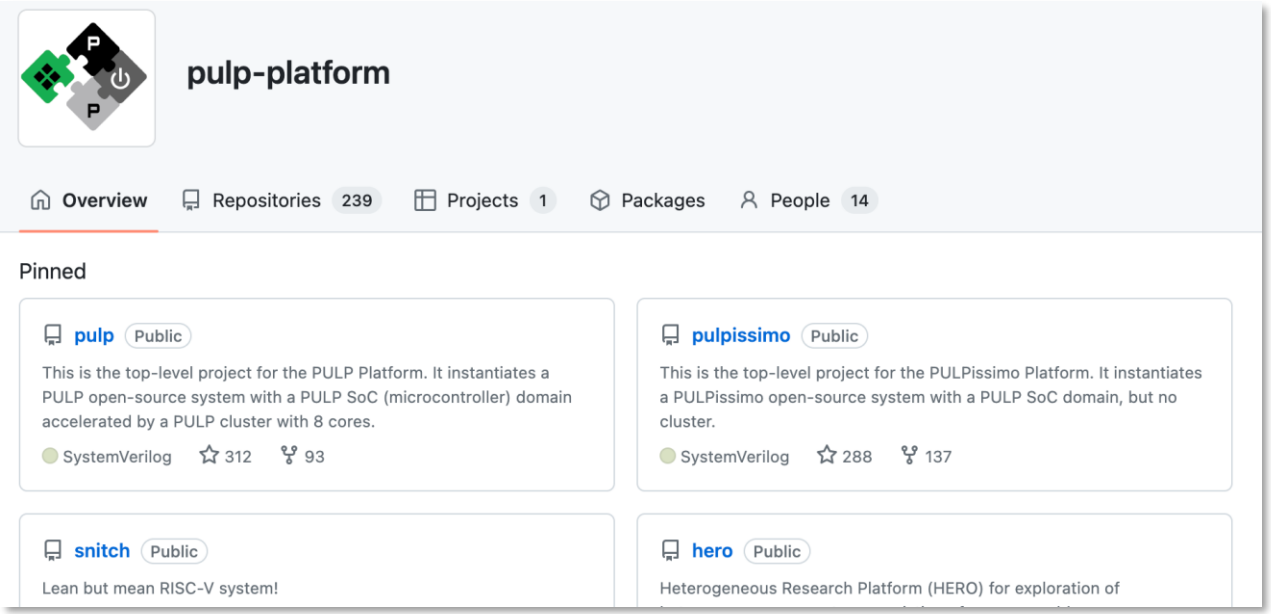
- **End-to-end open ASIC flow**
  - Students can take it **home** and **experiment** beyond the scope course
  - Transparent, approachable, **hackable**, more fine-granular
  - **Contribute** to the tools, flow, and library cells, further **improving** them
  - **Less bureaucracy** without NDAs

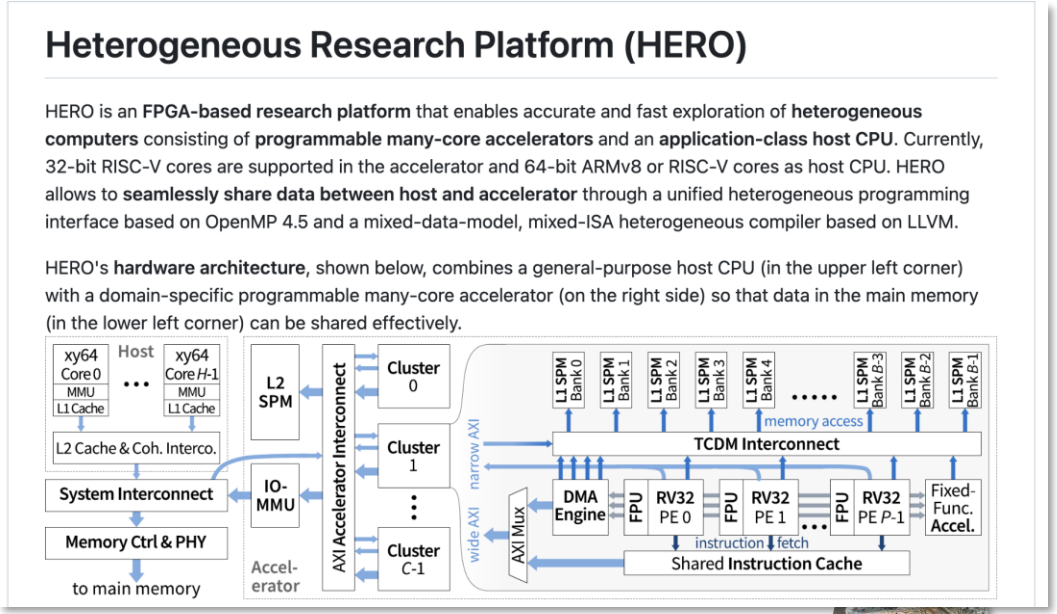
All Of Our Designs Are Open Source Hardware

- **All our development is on GitHub using a permissive license**
  - HDL source code, testbenches, software development kit, virtual platform

https://github.com/pulp-platform

- Allows anyone to use, change, and make products without restrictions.





Situation And Challenges

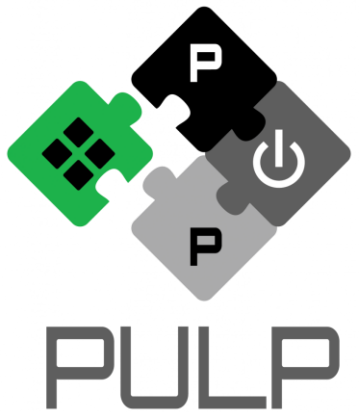
- **Open-source RTL established**
  - Led to a significant increase in hardware research output
  - Part of PULP's success

- **Open-source synthesis + backend**
  - Under development and advancing quickly
  - Established for simpler designs

- **What about European solutions?**
  - Build products from EU-based resources only

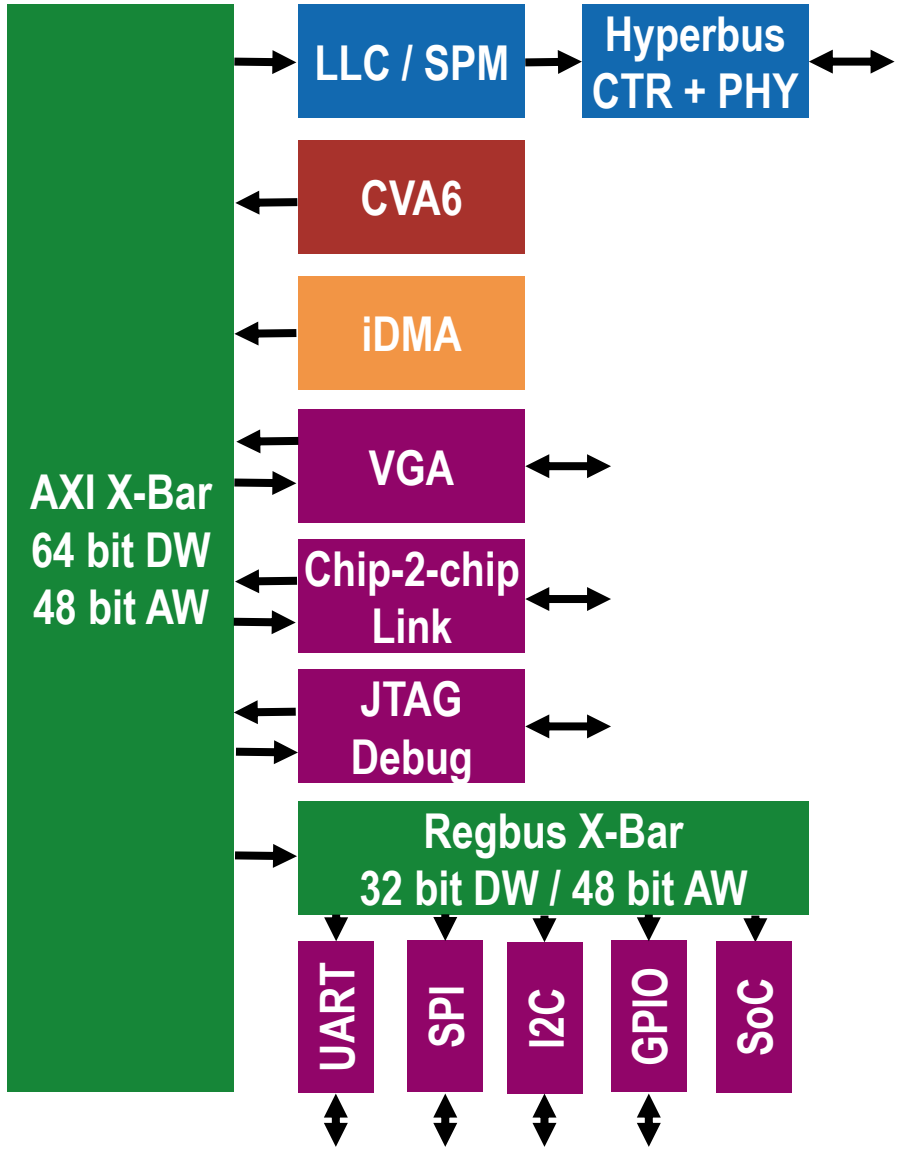
Our Contribution

- **Iguana, a demonstrator for the digital IHP13 flow**
  - Tapeout through Europractice in **July 2023**
  - **First end-to-end open-source ASIC** targeting to run **Linux**
  - Custom padframe allowing us complete control over IO
  - Improvements to the **tool, flow,** and open **design libraries**
- **Building Iguana from our open, industry-grade PULP IPs**
  - **Cheshire** SoC framework
  - Including **2 fully digital off-chip** interfaces
    - HyperBus and chip-to-chip link
- **Large team of 14 people for the Iguana Design**
  - 7 undergrad students (in 4 sub-projects), 4 PhDs, 3 staff from DZ, (5 FTE)
  - Support of many more from the PULP team



Iguana's Architecture

- **CVA6: RV64GC**
  - Created at IIS, maintained by OpenHW group
- **AXI4 and Regbus used in interconnect**
- **AXI4-based last-level cache / SPM**
- **Peripherals**
- **Standalone boot**
  - SPI (SD Card – GPT)
  - I2C
- **Open-source, digital-only, PHYs**
  - HyperBus off-chip memory interface
  - Chip-2-Chip link



Off-Chip Fully Digital PHYs

- **HyperBus DRAM interface**
  - **Automotive standard** to connect **off-chip RAM** and flash
  - **11 signals** only; multiplexed command, address, data bus
  - Rigorous requirements on those 11 pins
    - Inverted clock pair
    - 8 parallel DDR data channels
    - Bidirectional strobe signal
  - Internally: 2 programmable **delay lines**

`github.com/pulp-platform/hyperbus`

- **Digital chip-to-chip link**
  - Our in-house design, digital-only, GPIO pads
  - Configurable amount of parallel lines
  - Source-synchronous clocks

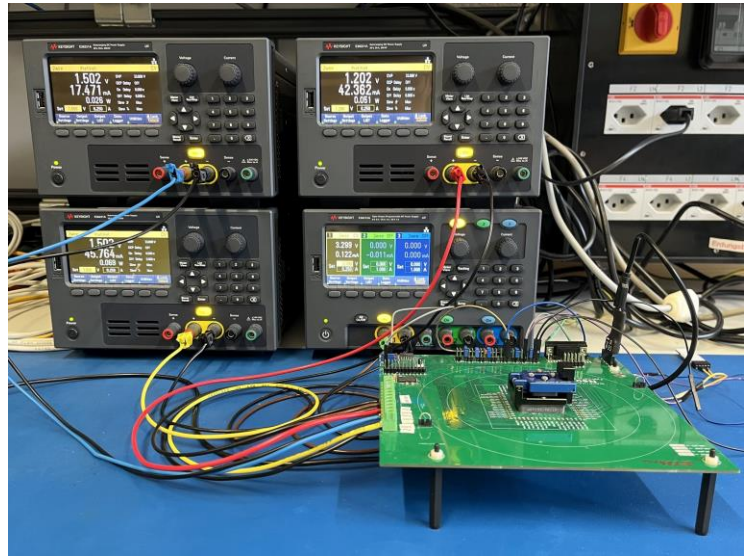
`github.com/pulp-platform/serial_link`

The Cheshire Concept & Silicon Demonstrator

- **Iguana is built using Cheshire**
  - **Silicon-proven** Linux SoC framework, FPGA port
  - Parametrizable top

`github.com/pulp-platform/cheshire`

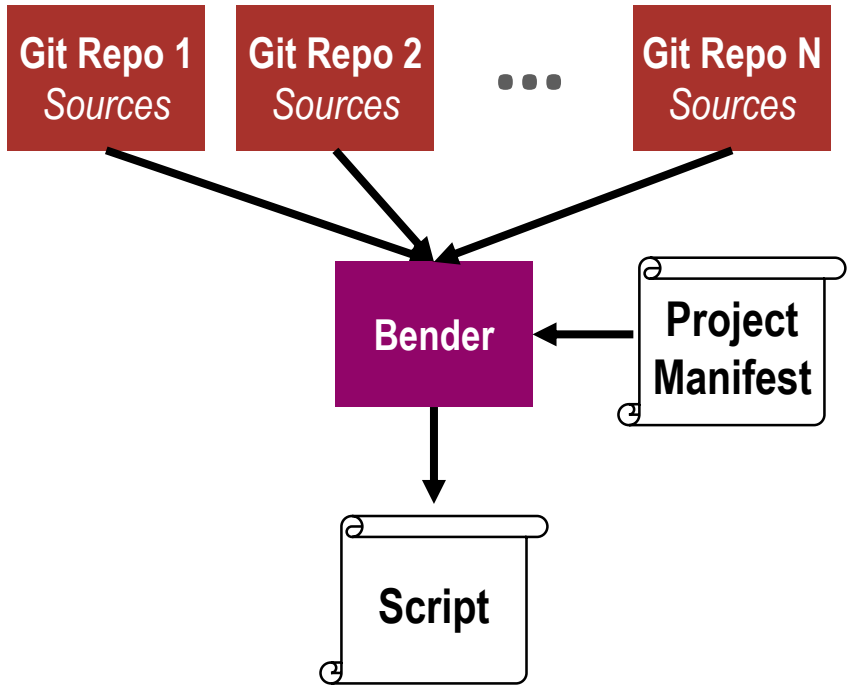
- **Silicon Demonstrator**
  - Neo student **tapeout** in 2022
  - TSMC 65nm node, closed toolchain
  - Similar SoC, different DRAM controller
  - Tested and is **working standalone** ☺



Ottaviano, Alessandro, et al. "**Cheshire: A Lightweight, Linux-Capable RISC-V Host Platform for Domain-Specific Accelerator Plug-In**“,
IEEE Transactions on Circuits and Systems Part II: Express Briefs, 2023

Our Flow: In-house Tools

- **Bender**
  - Source and dependency management
  - Script generation
  - Similar to FuseSoC
    - **Resolve project dependencies**
- **Morty**
  - **Source pickler** → single file, single context
  - Macro expansion
- **SVase**
  - Parameter and generate **pre-elaboration**
  - Human-readable simplification of SV
  - It uses the *slang* SystemVerilog parser

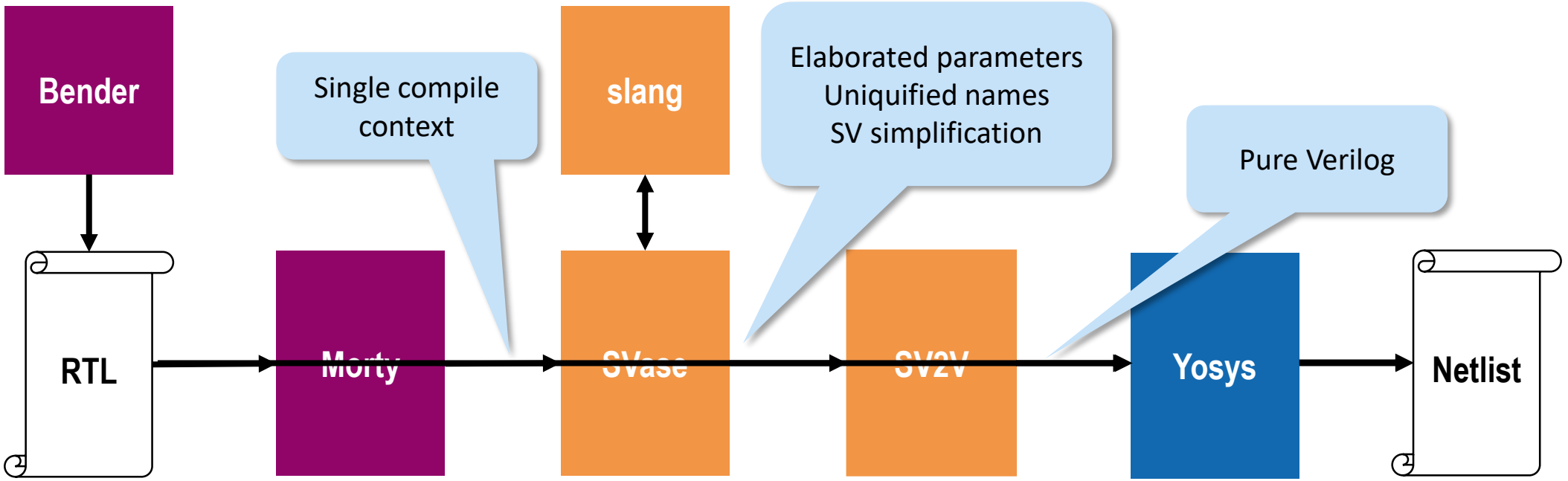


github.com/pulp-platform/bender

github.com/pulp-platform/morty

github.com/pulp-platform/svase

Frontend: RTL to Netlist



- **Bender and Morty** to handle RTL sources
- **SVase** parameter elaboration & simplification
- **SV2V** to transform the remaining SV constructs
- **Yosys** synthesis

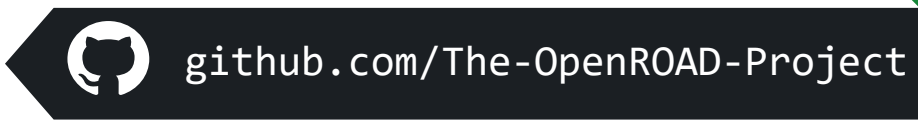
github.com/pulp-platform/svase

github.com/zachjs/sv2v

github.com/YosysHQ/yosys

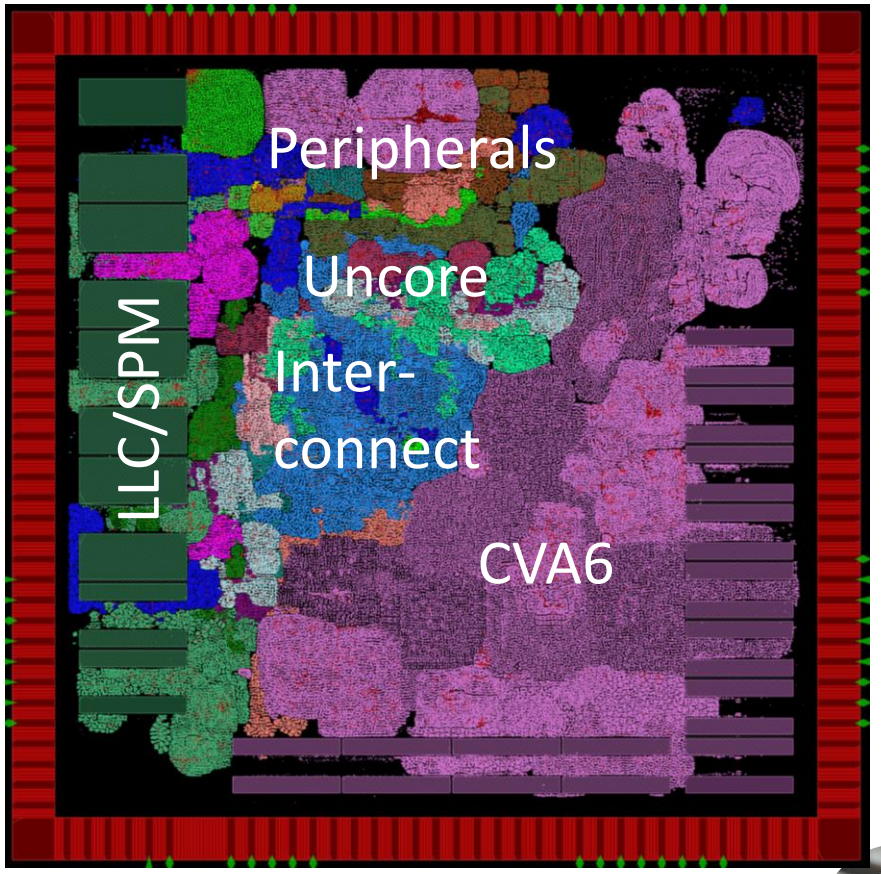
Backend

- **OpenROAD and Klayout**

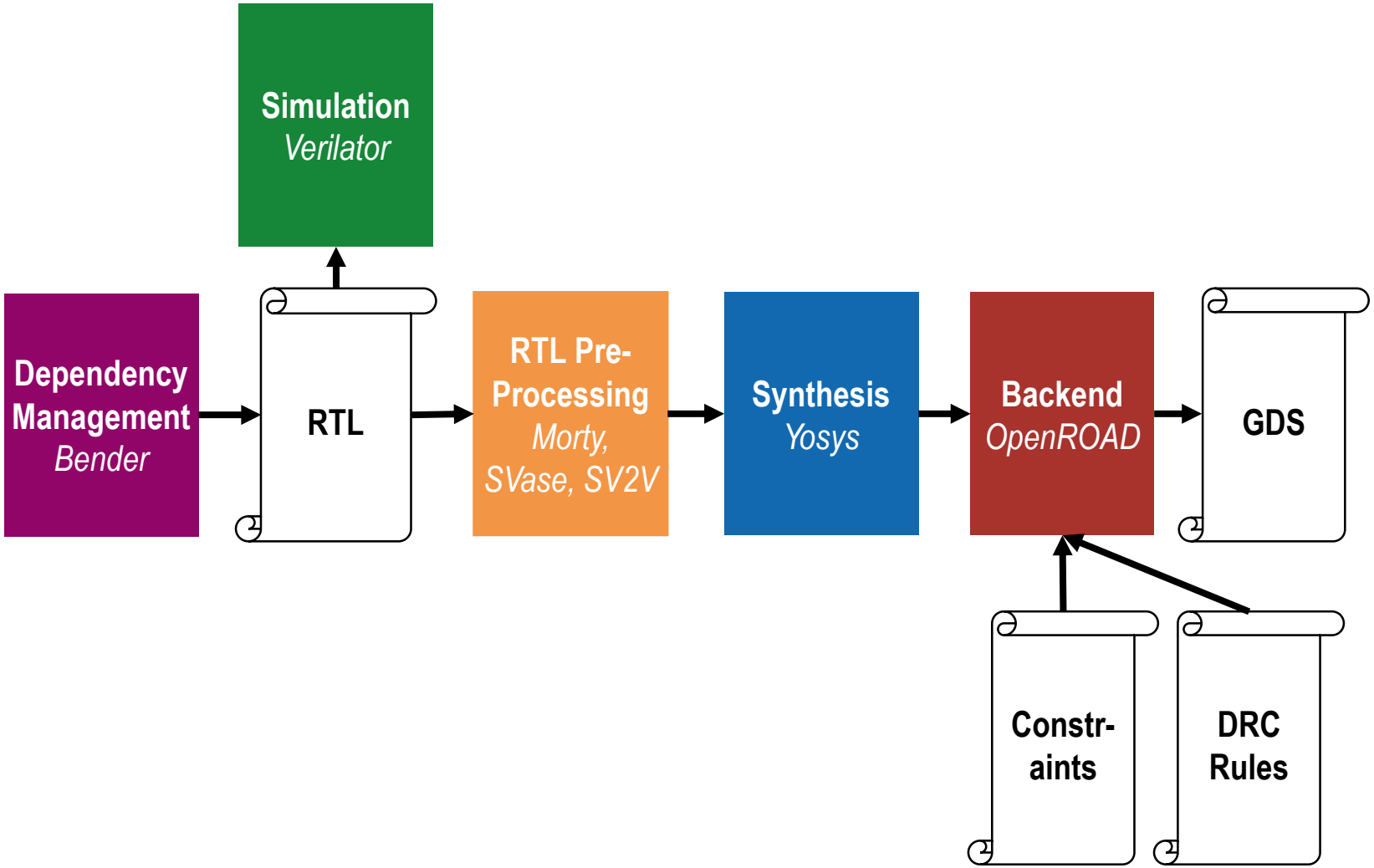


- **Custom TCL-only flow**
  - Based on our traditional flow called “**cockpit**”
  - **Simpler**, in line with our **teaching**
  - Tool and technology knowledge from *OpenROAD Flow* scripts

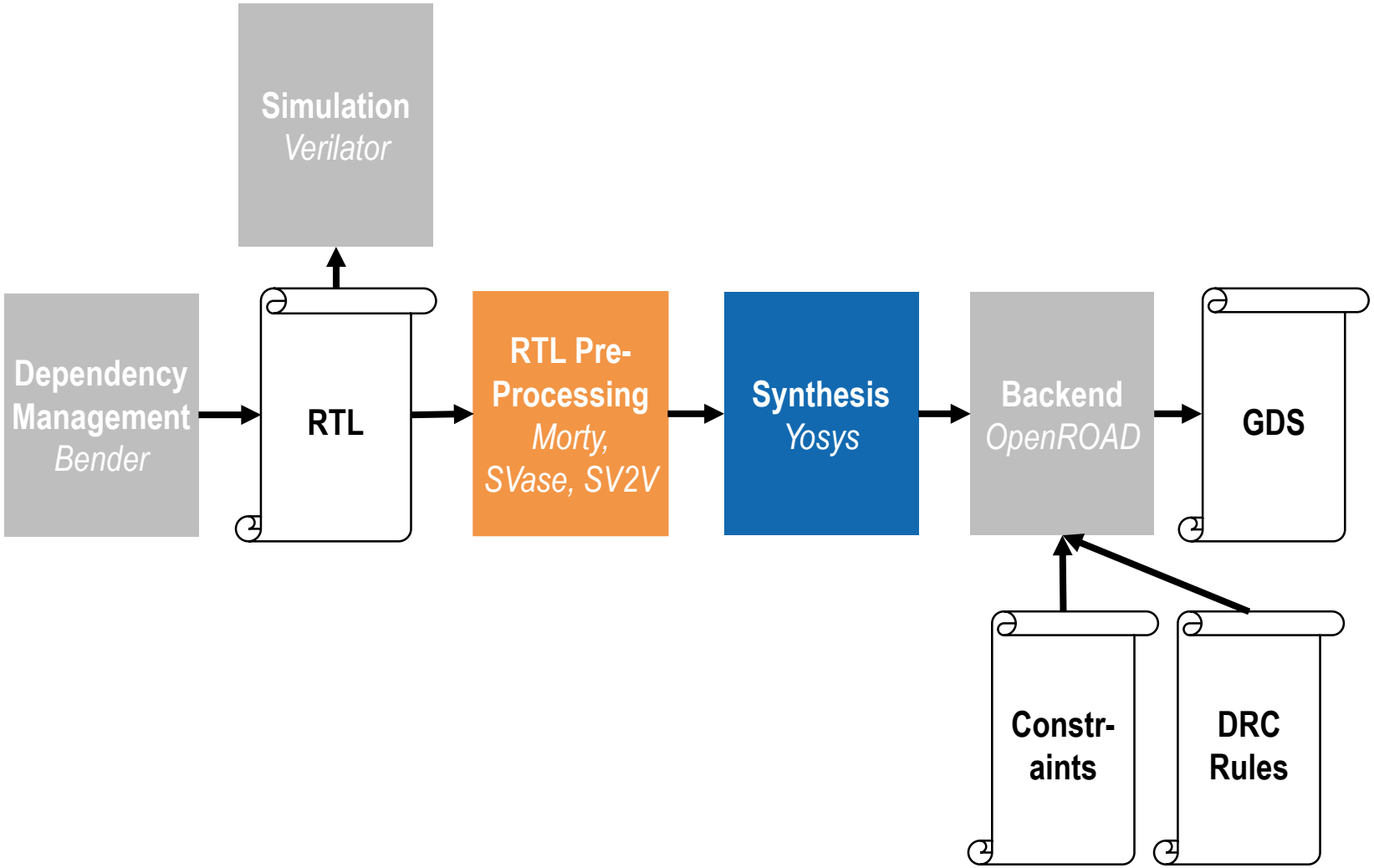
- **Flat implementation**
  - **Manageable turnaround** time, no hierarchy needed
  - Most of the area is occupied by **CVA6**
  - **6.2 x 6.2 mm**



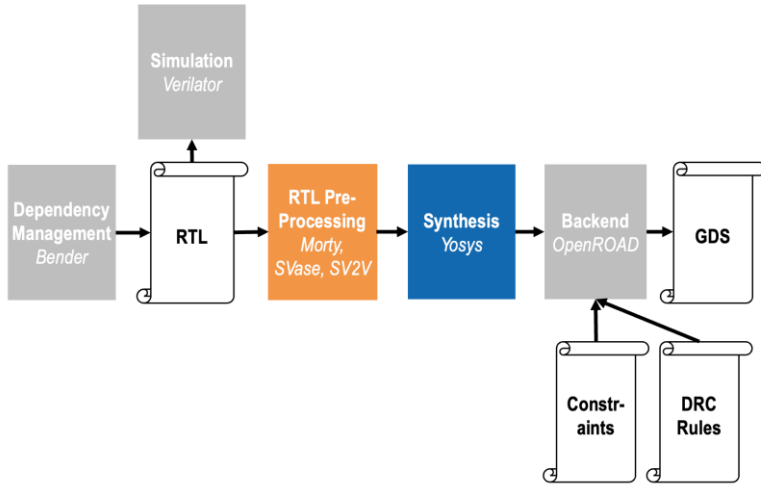
Overview Of Our Current Flow



Focus: Synthesis

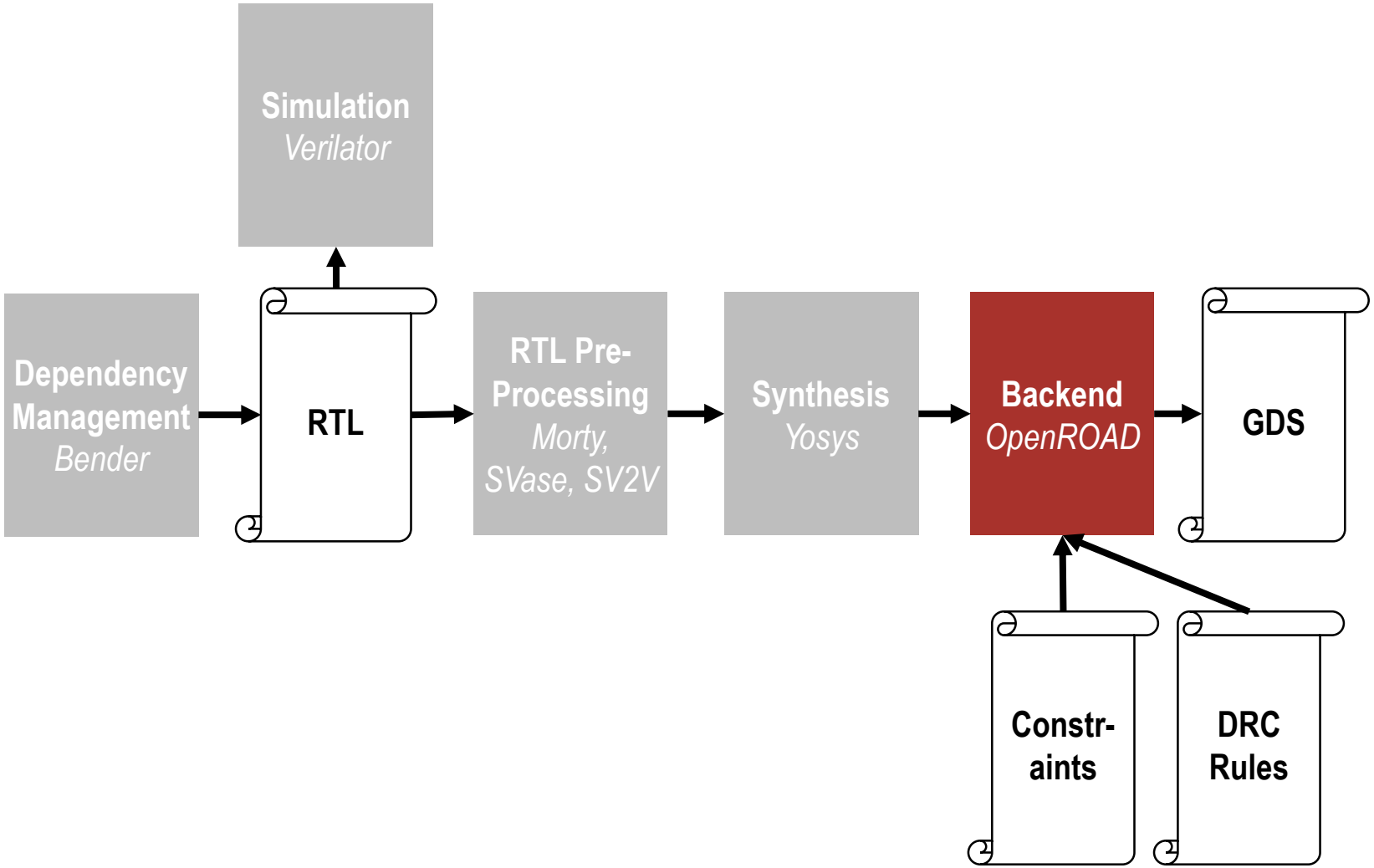


Wishlist and Difficulties - Synthesis

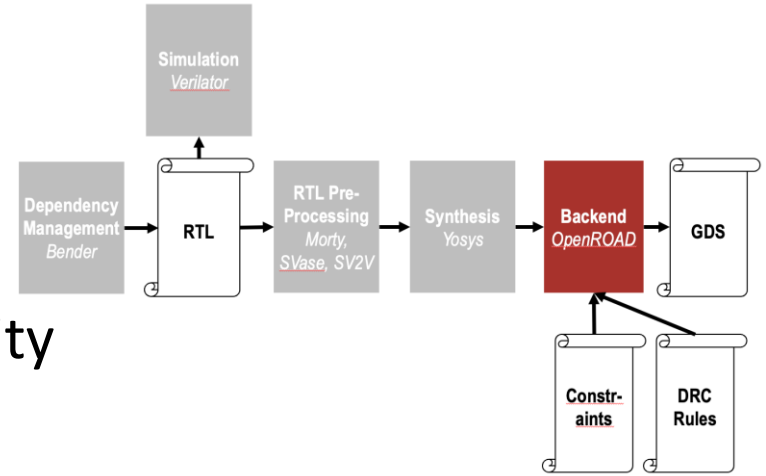


- **More challenging** than the backend
- Synthesis can be improved
  - **LSOracle** improves our QoR only by a few %
  - Missing library of optimized blocks (multiplication)
  - Standard cell memory and ROMs scale poorly
- Generally, the **RTL frontend is less mature** in the open domain
  - Industry-grade SystemVerilog **too sophisticated** for Yosys
  - Our assessment: SV2V > Surelog UHDM plugin > native Yosys
- **Slang** has very good Lexing, Parsing, and *Elaboration*
  - **SVase** is one of the first tools using it
  - Ideally: use it directly as a frontend

Focus: Backend

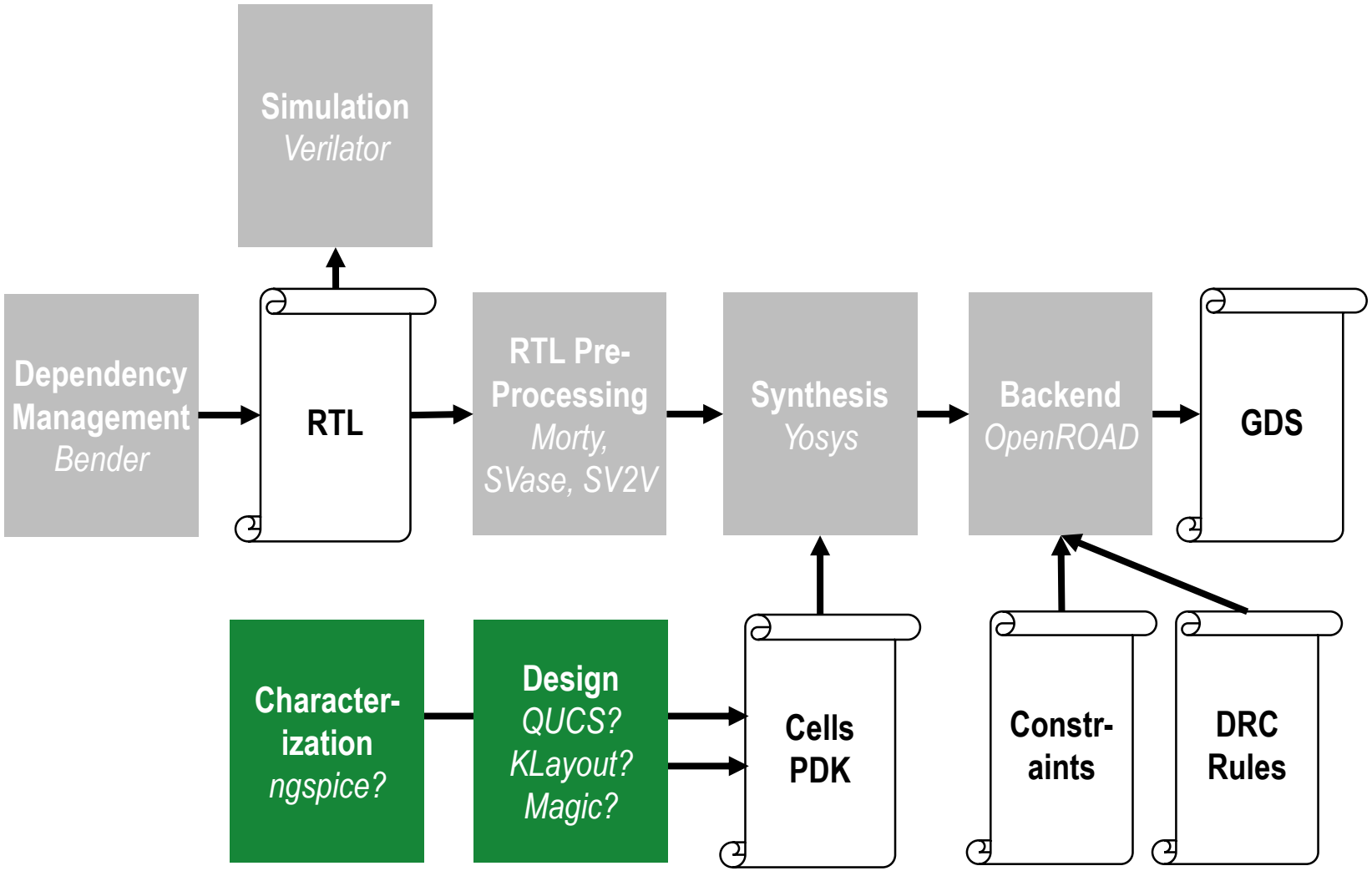


Wishlist and Challenges - Backend



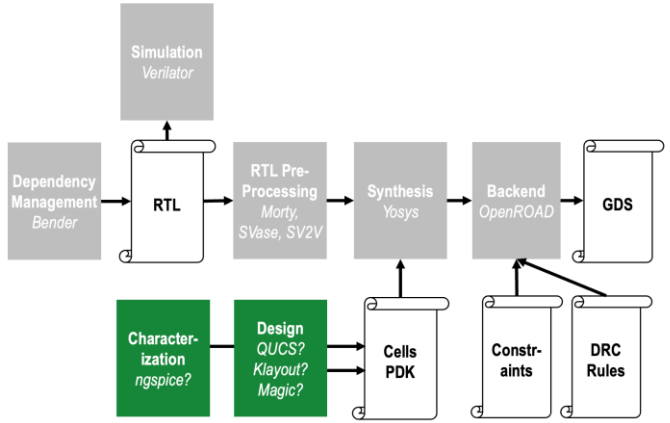
- The backend is **very solid**
- **OpenROAD** has an enormous development velocity
  - Insufficient versioning
  - Since mid-April 2023, over **1000+** commits!
- Some tuning is needed per technology
  - We added some **IHP13-specific** changes
  - More is required to **improve QoR** further
- Features that are currently lacking:
  - Antenna rule fixing (works for other PDKs but not for IHP)
  - DRC fixing works but is not perfect
  - DRV, we had a lot of max cap violations

The (perfect) Open Flow for the Future - Cells



Wishlist – PDK and Cells

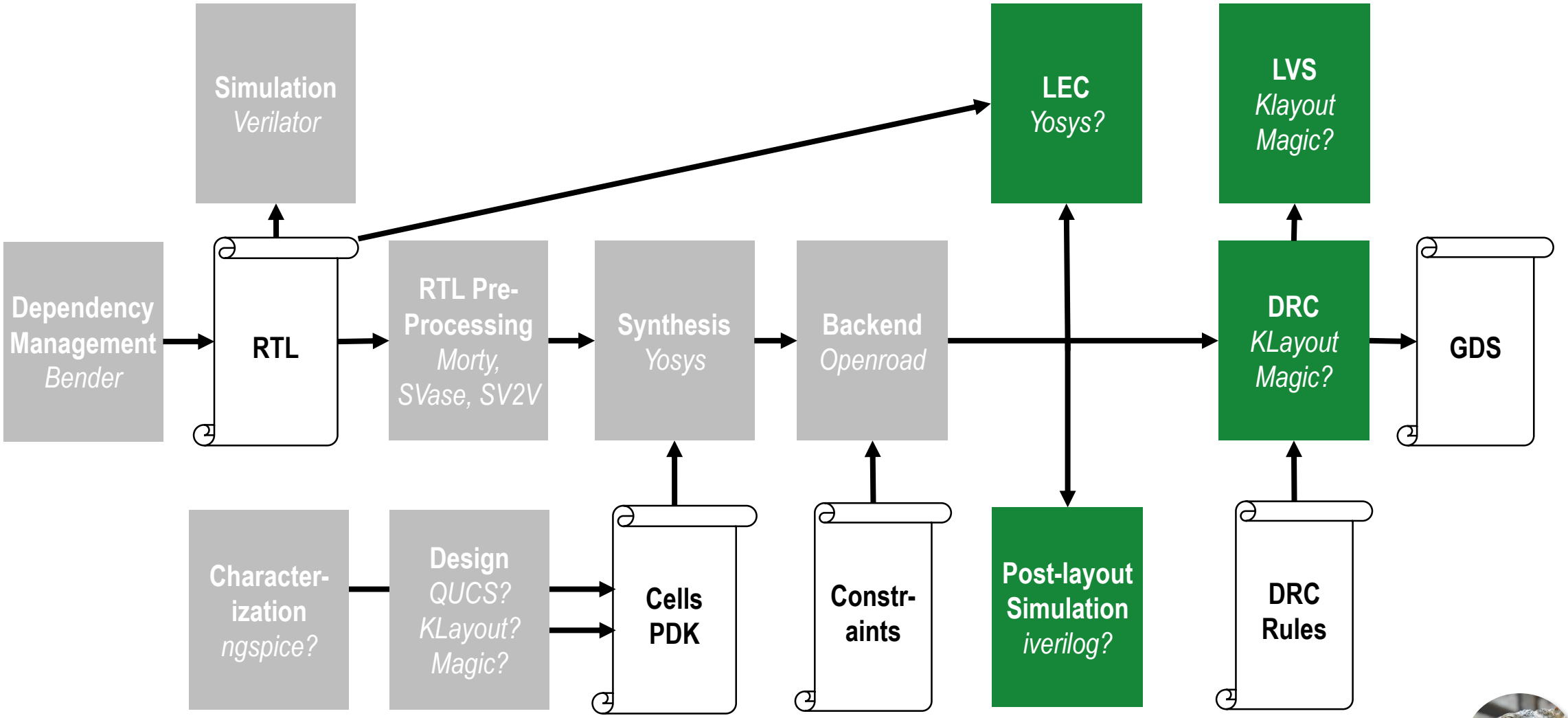
- Let the **community** take part in it!
  - We organized **two** Hackathons
    - **Undergrad** students can easily contribute
  - More **specialized** cells improve QoR
  - Opens **new** doors
    - Research and Education
- How can we make this possible?
  - **GitHub** is an excellent decision; moderation is needed
  - What is missing: **design and evaluation** environment
    - **Quick** turnaround times are critical; estimations would be fine
    - QUCS, Magic, and KLayout to draw the cells
    - ngspice for characterization?
    - Part of the analog roadmap?



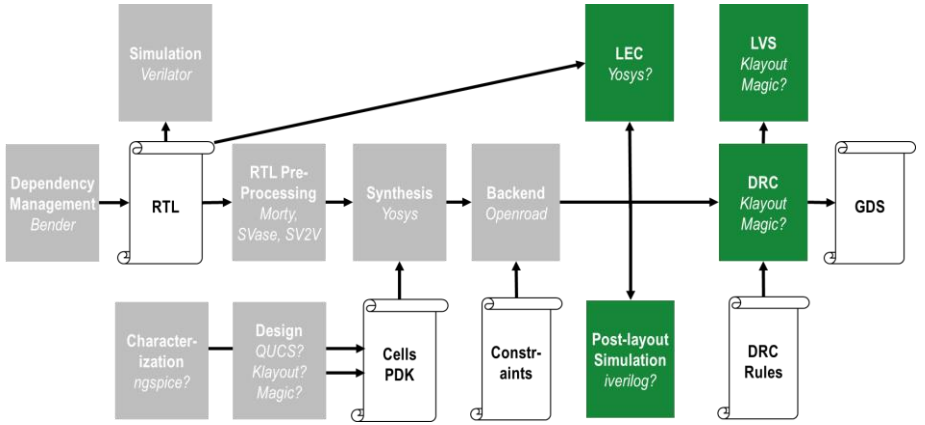
Note. Adapted from photo taken by Frank at standard cell hackathon. May 13th, 2023

Hochschule RheinMain

The (perfect) Open Flow for the Future - Verification



Wishlist - Verification

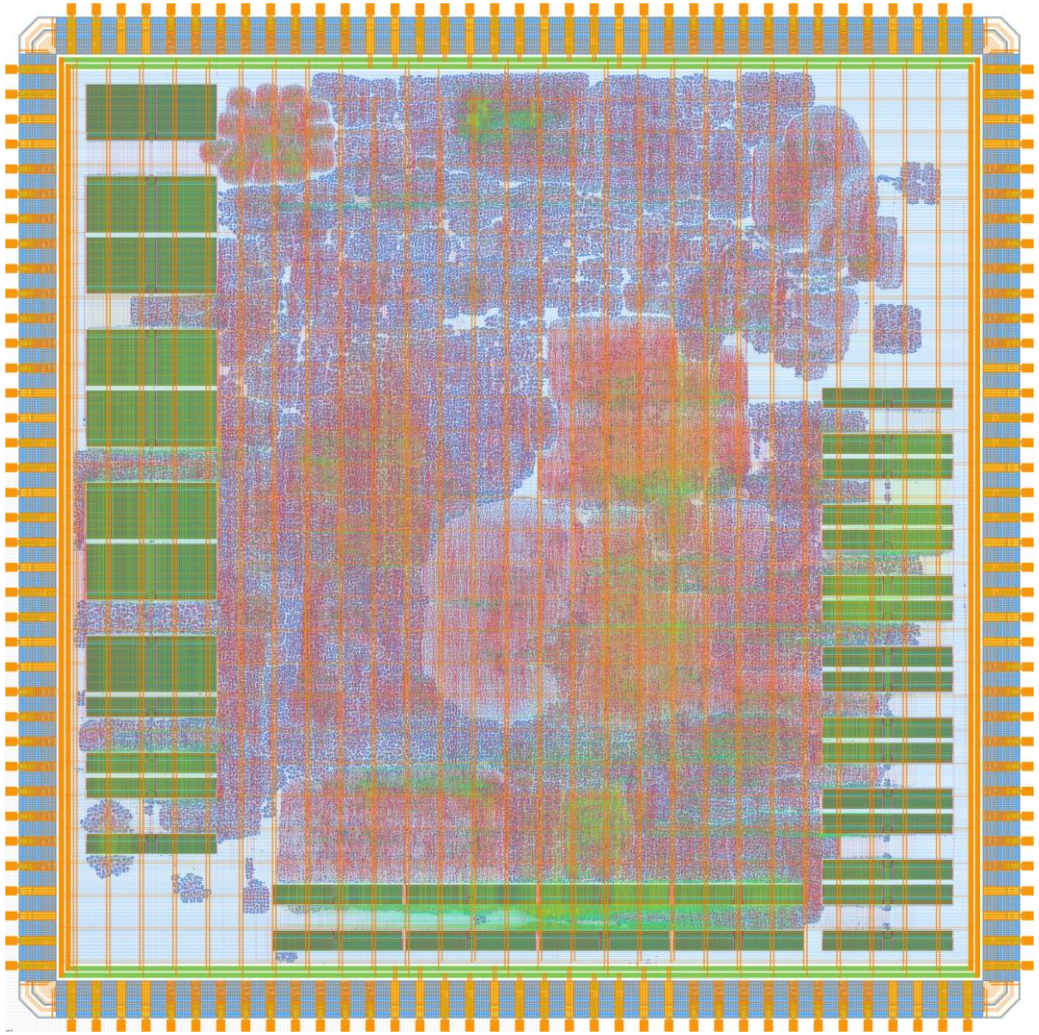


- **Everyone wants to design**
  - Verification is not as popular, but **essential**!
- **Logic equivalency check (LEC)**
  - **Complicated** chain of tools, many steps
  - Tools in the chain need to **assist** LEC
- **DRC / LVS**
  - KLayout or Magic?
  - **How** to describe rules?
- **DFT**
  - Fault? – part of OpenLane
- **Annotated Post-layout Simulation**
  - We could not get iverilog to run with our design

Deliverables

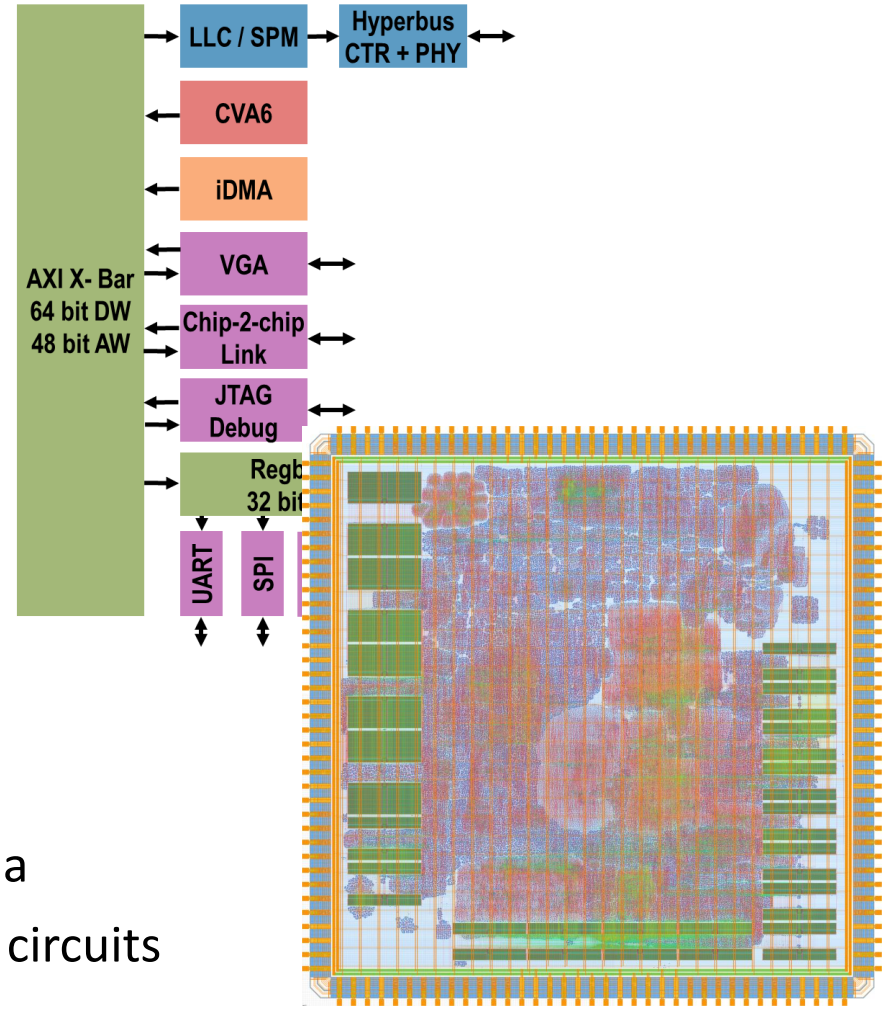
- **Targeting fully-open GDS**
  - The path for open standard cells is clear
  - What about SRAM macros and I/O Cells?
  - 40mm^2 in IHP 130nm
  - > 75 MHz (WC, conservative)

- **Immediate next steps:**
  - **Releasing our flow**
  - **Turnkey** Iguana implementation
  - How do we handle SRAMs and IO cells? **LEF**?
  - Docker?



Conclusion and Outlook

- **Linux-capable RV64GC RISC-V SoC**
- **Open off-chip DRAM and chip-2-chip link**
- **Industry-grade SystemVerilog IPs**
- **OpenROAD backend with “cockpit” flow**
- **Tapeout through Europractice in July 2023**
  - **Assess and establish open** flow for complex designs
- Experience involving **undergrad** students
- **Future Tapeouts are planned**
  - Tegu and Komodo: will build upon and **extend** Iguana
  - Multicore CVA6, real-time SoC, aging, and reliability circuits



PULP Platform

Open Source Hardware, the way it should be!

Thomas Benz tbenz@iis.ee.ethz.ch
Paul Scheffler paulsc@iis.ee.ethz.ch
Jannis Schönleber janniss@iis.ee.ethz.ch

github.com/pulp-platform/iguana

Institut für Integrierte Systeme – ETH Zürich
Gloriastrasse 35
Zürich, Switzerland

DEI – Universitá di Bologna
Viale del Risorgimento 2
Bologna, Italy

@pulp_platform

pulp-platform.org

youtube.com/pulp_platform

ETH zürich ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA