

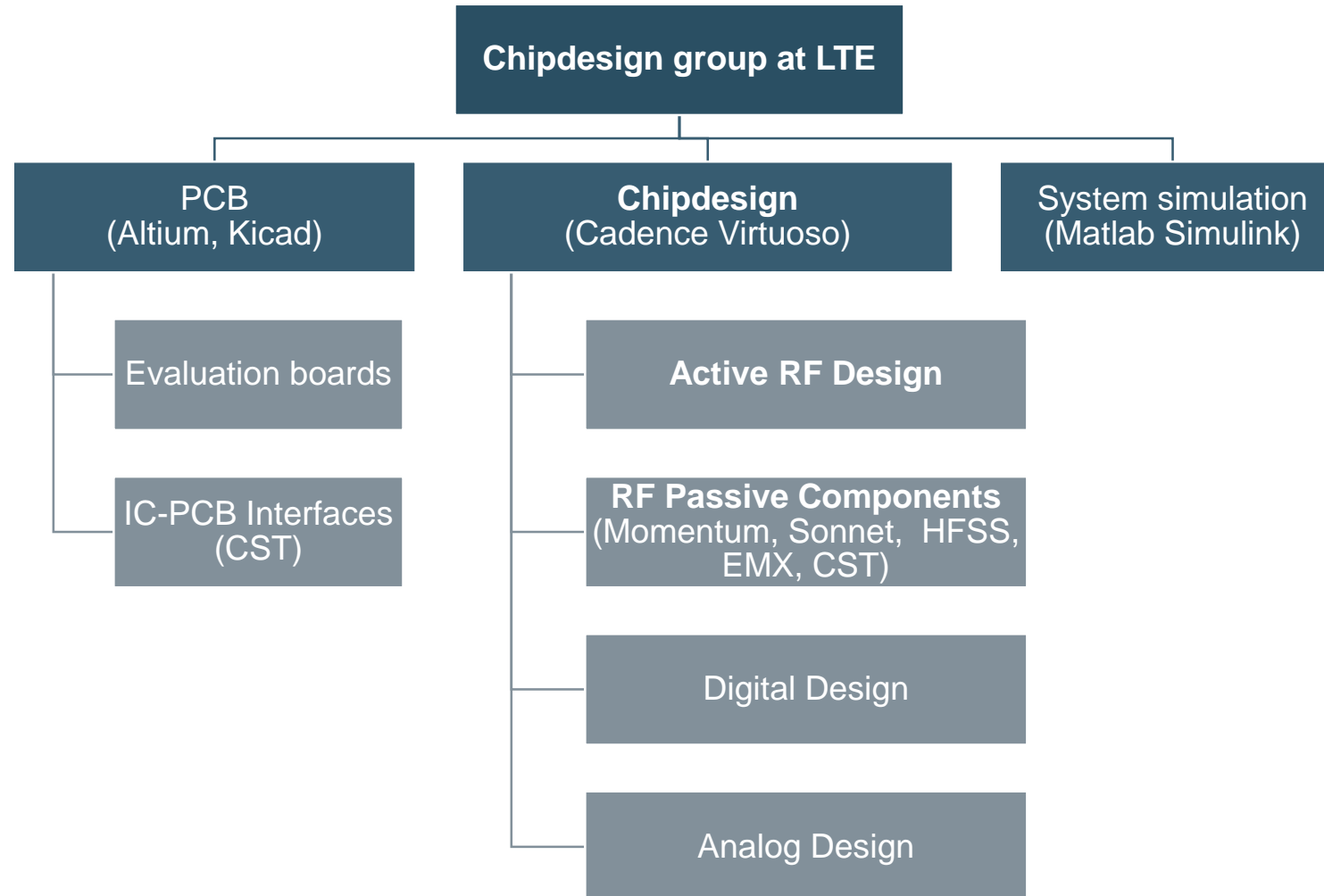
Design-flow approaches for mmWave and sub-THz integrated transceiver circuits for radar and communication

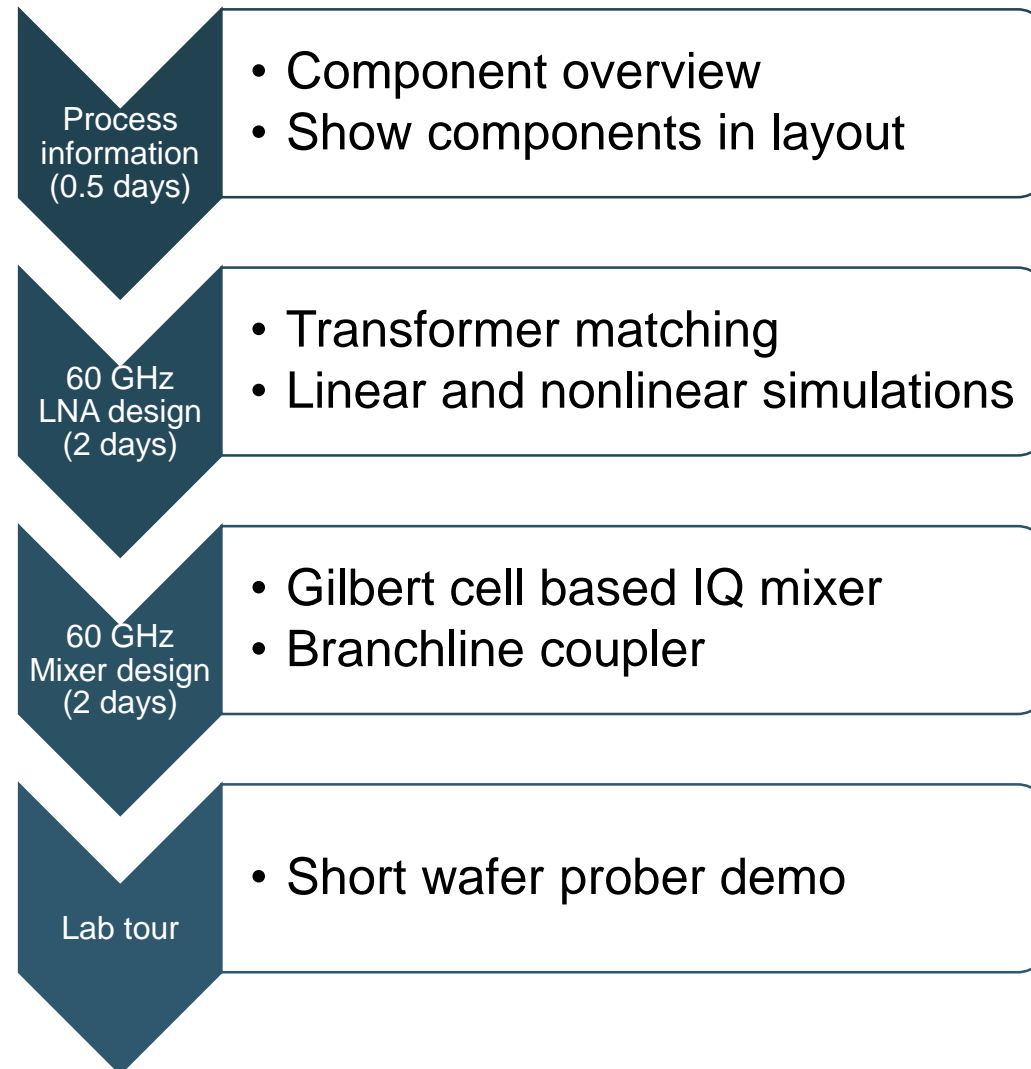
From a design tools user perspective

Manuel Koch

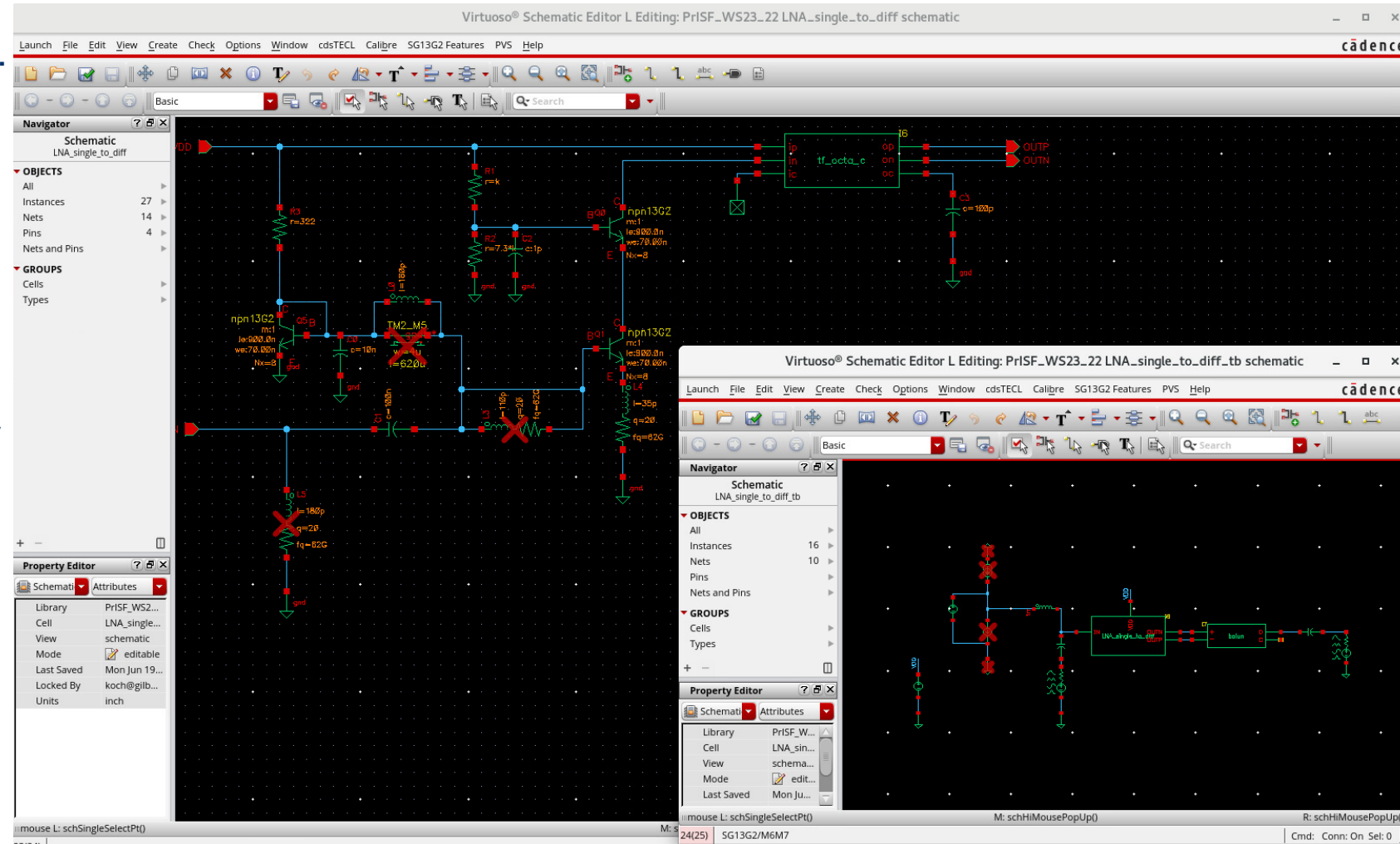
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- 01 Design Tools Overview
- 02 Design Example – Student lab course circuits
- 03 Layout Creation
- 04 Auxiliary Circuits
- 05 Library Management
- 06 Summary

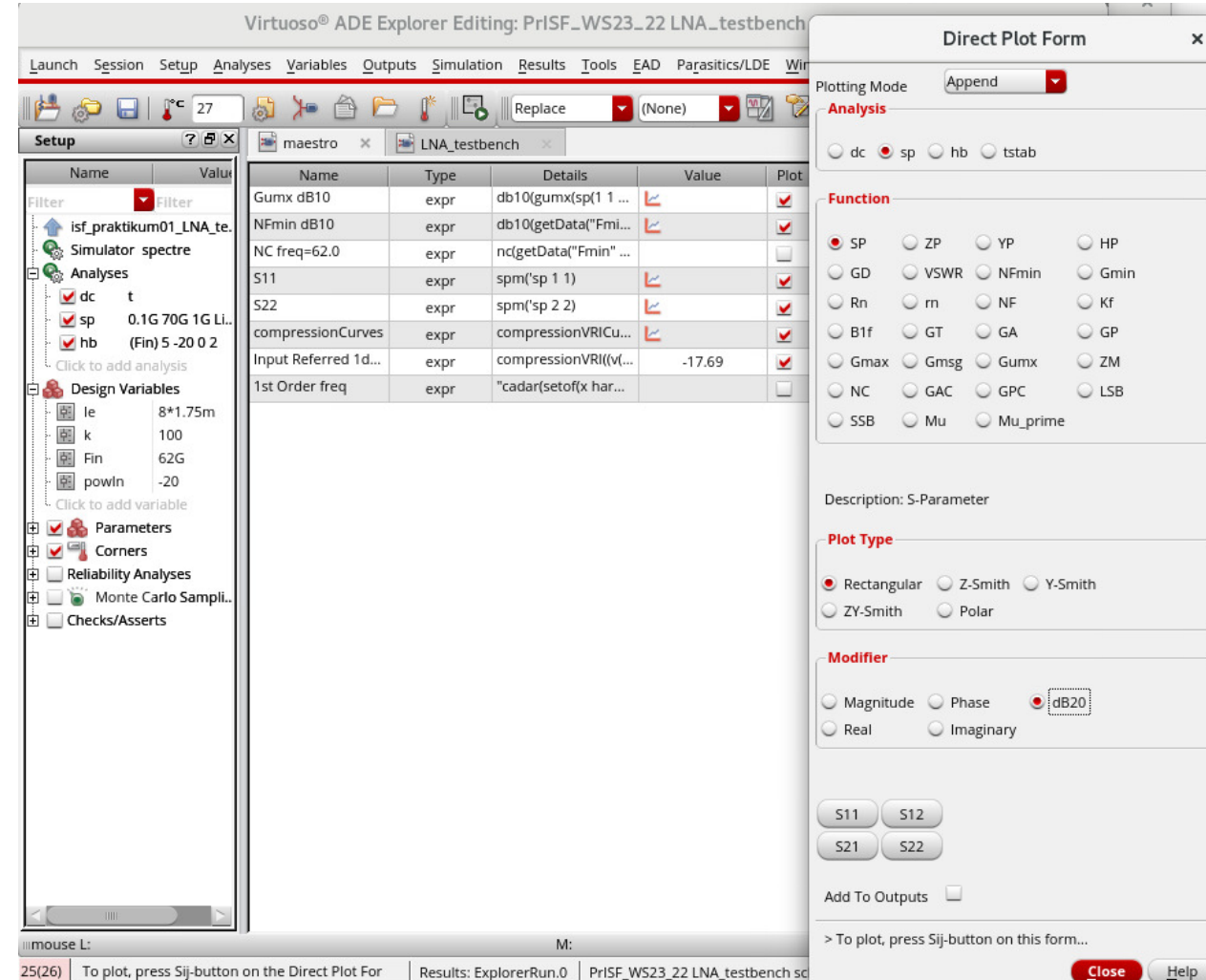




- HBTs, Resistors, Capacitors...
- Transmission Lines
 - PDK models
 - Cadence rfTLineLib
- Inductors and Transformers
 - Ideal Components with Q factor
 - EM Simulated Structures
- Testbench
 - Sources, ideal balun, ...



- S-parameter / Z-parameter simulation
- Differential mode, common mode, ...
- Noise simulation
- Harmonic Balance / Periodic steady state
- Noise simulation
- Large signal S-parameter
- Intermodulation
- Transient simulation



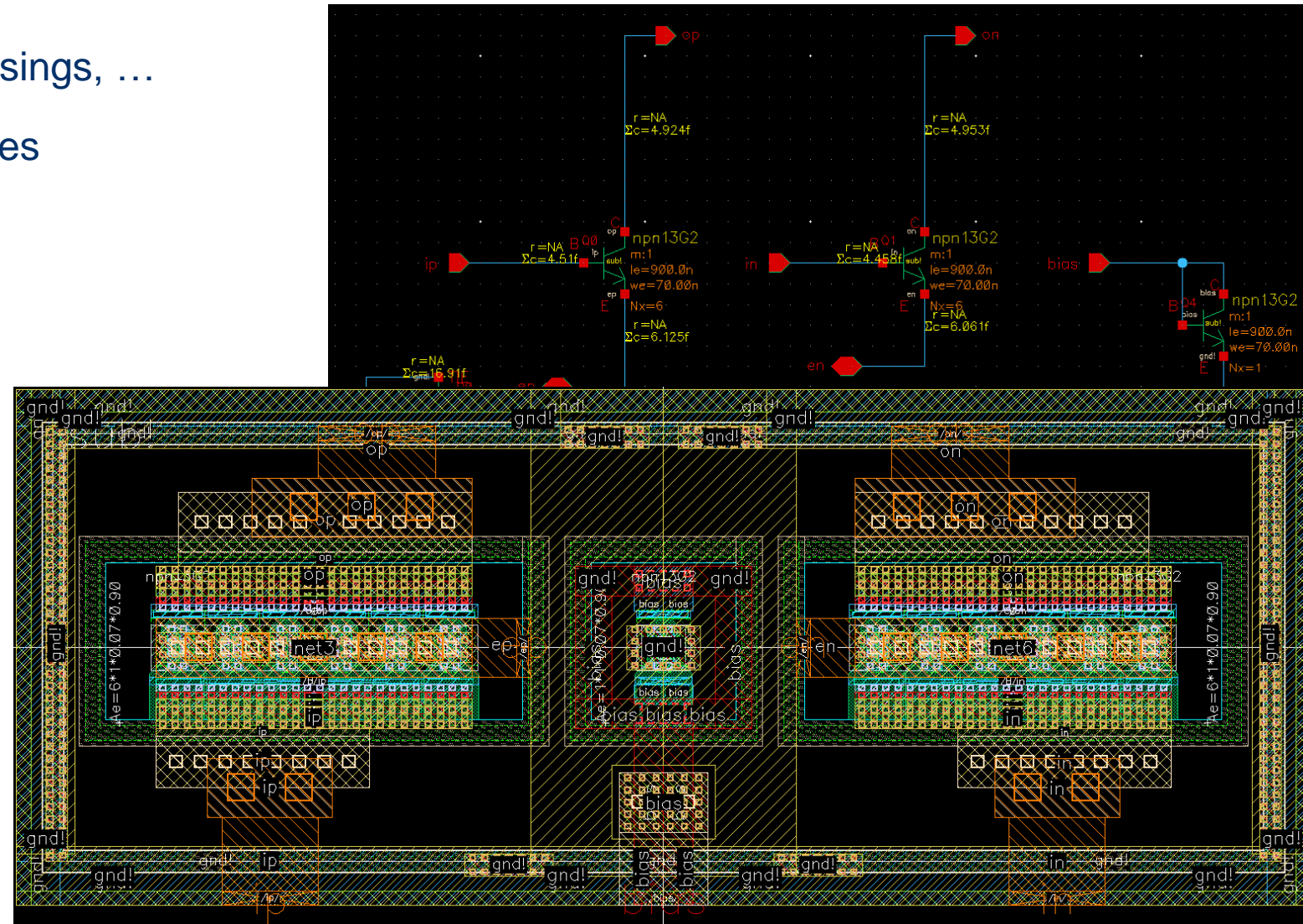
The screenshot displays the Virtuoso ADE Explorer interface for a simulation project named 'PrISF_WS23_22 LNA_testbench'. The main window shows a 'Setup' panel on the left with a tree view of simulation settings, including 'Analyses' (dc, sp, hb) and 'Design Variables' (le, k, Fin, powIn). The central pane shows a table of simulation results:

Name	Type	Details	Value	Plot
Gumx dB10	expr	db10(gumx(sp1 1 ...		<input checked="" type="checkbox"/>
NFmin dB10	expr	db10(getData("Fmi...		<input checked="" type="checkbox"/>
NC freq=62.0	expr	nc(getData("Fmin" ...		<input type="checkbox"/>
S11	expr	spm('sp 1 1)		<input checked="" type="checkbox"/>
S22	expr	spm('sp 2 2)		<input checked="" type="checkbox"/>
compressionCurves	expr	compressionVRIcu...		<input checked="" type="checkbox"/>
Input Referred 1d...	expr	compressionVRI(v(...	-17.69	<input checked="" type="checkbox"/>
1st Order freq	expr	"cadar(setof(x har...		<input type="checkbox"/>

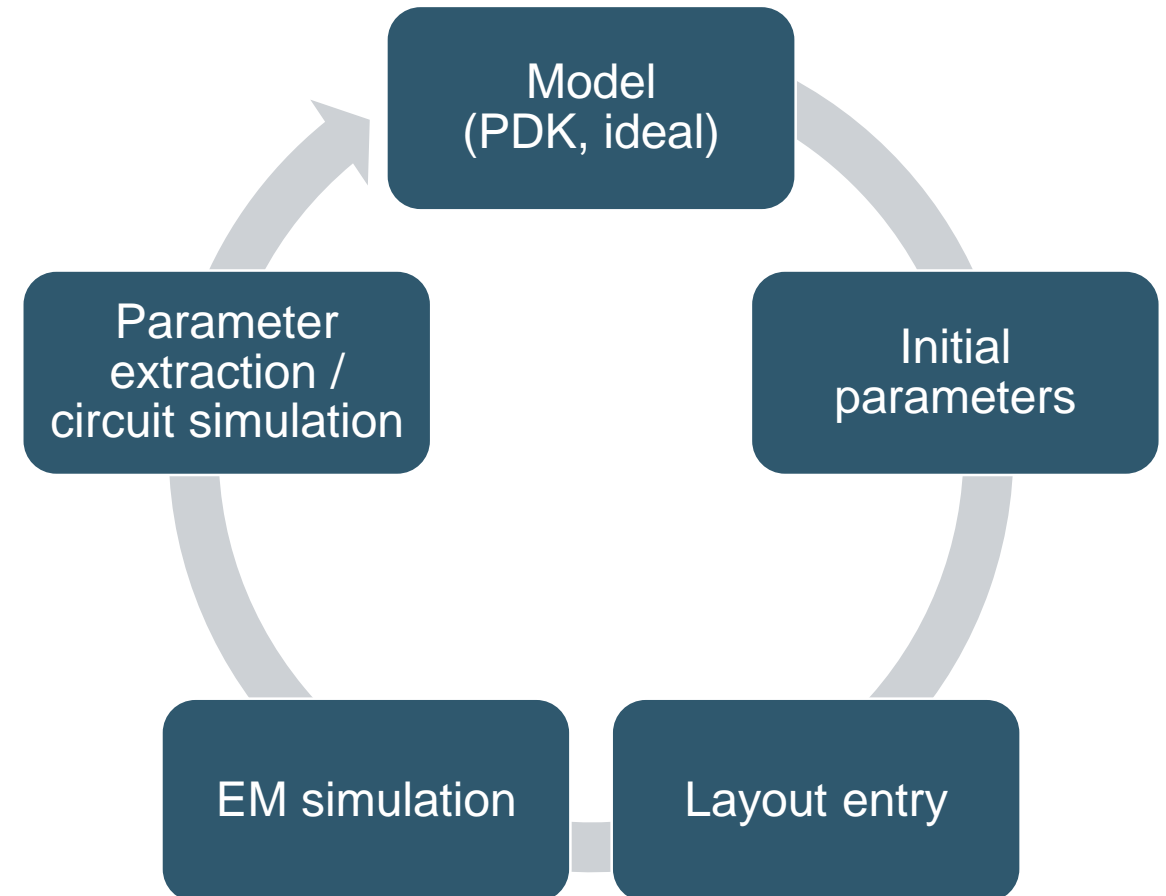
Overlaid on the right is the 'Direct Plot Form' dialog box. It is configured for 'Plotting Mode' set to 'Append' and 'Analysis' set to 'sp'. The 'Function' section has 'SP' selected. The 'Plot Type' section has 'Rectangular' selected. The 'Modifier' section has 'dB20' selected. The 'Description' is 'S-Parameter'. Buttons for 'S11', 'S12', 'S21', and 'S22' are visible. At the bottom, there are 'Close' and 'Help' buttons.

Layout – Core Cells

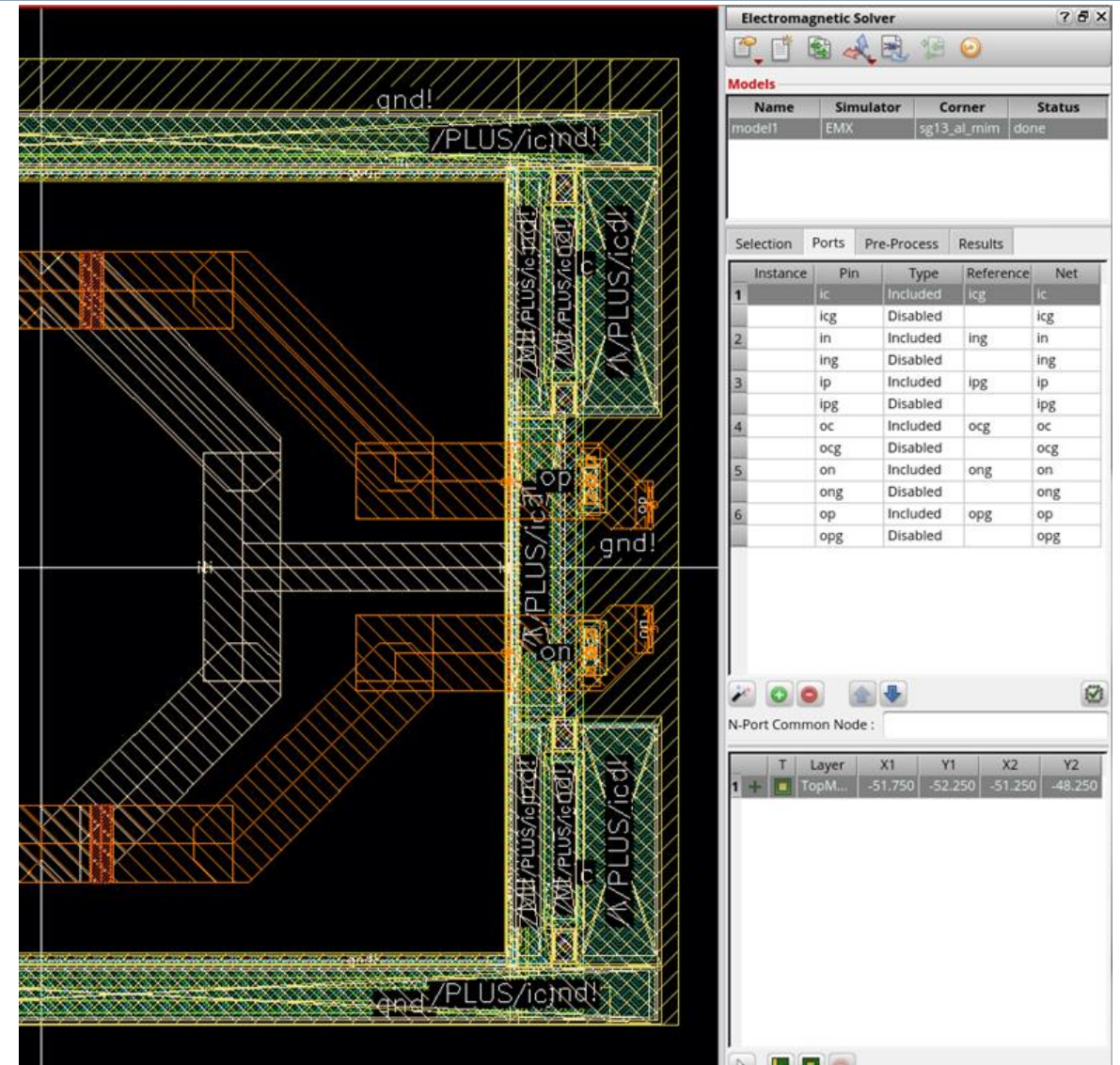
- Small cell with Transistors, Vias, Crossings, ...
- Layout with Transmission line interfaces
- Parasitic Extraction (C, RC)
- Annotation in schematic



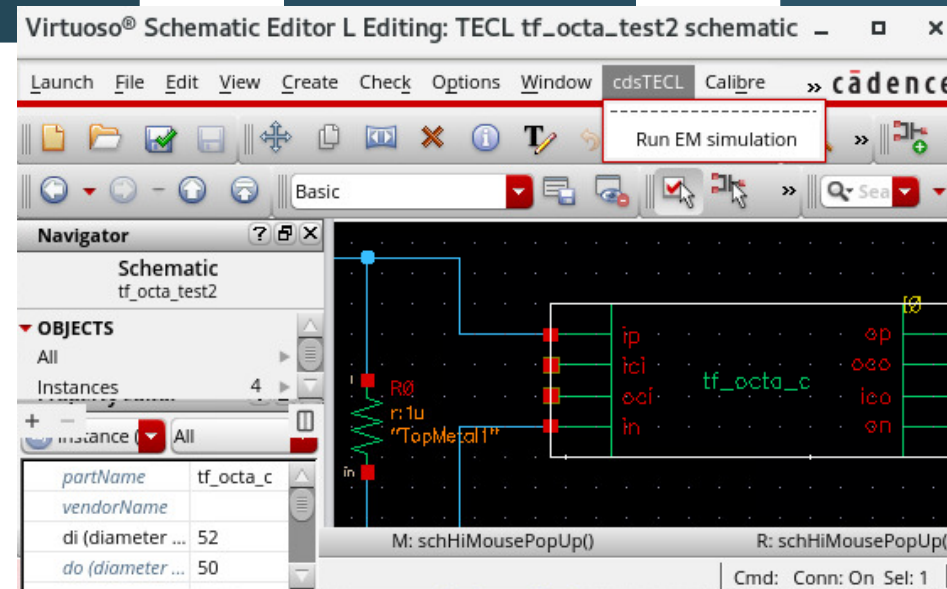
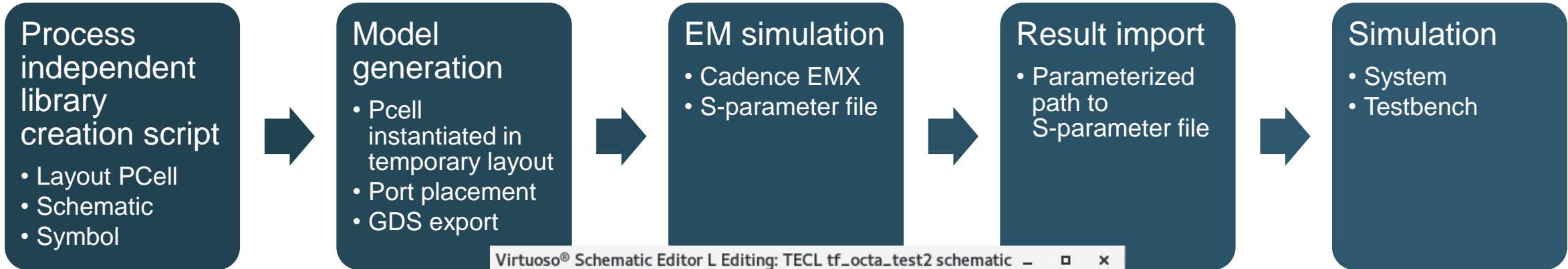
- Transmission lines, inductors, transformers, Lange coupler, Baluns, slow wave lines, ...
- Testbenches e.g. for inductance and quality factor extraction
- S-parameter best to be saved in design library
- Coupling effects of multiple passive components
- Speeding up the cycle:
 1. Saved simulation settings, automatic pin adjustment
 2. Parametric models
 3. Automated EM simulation



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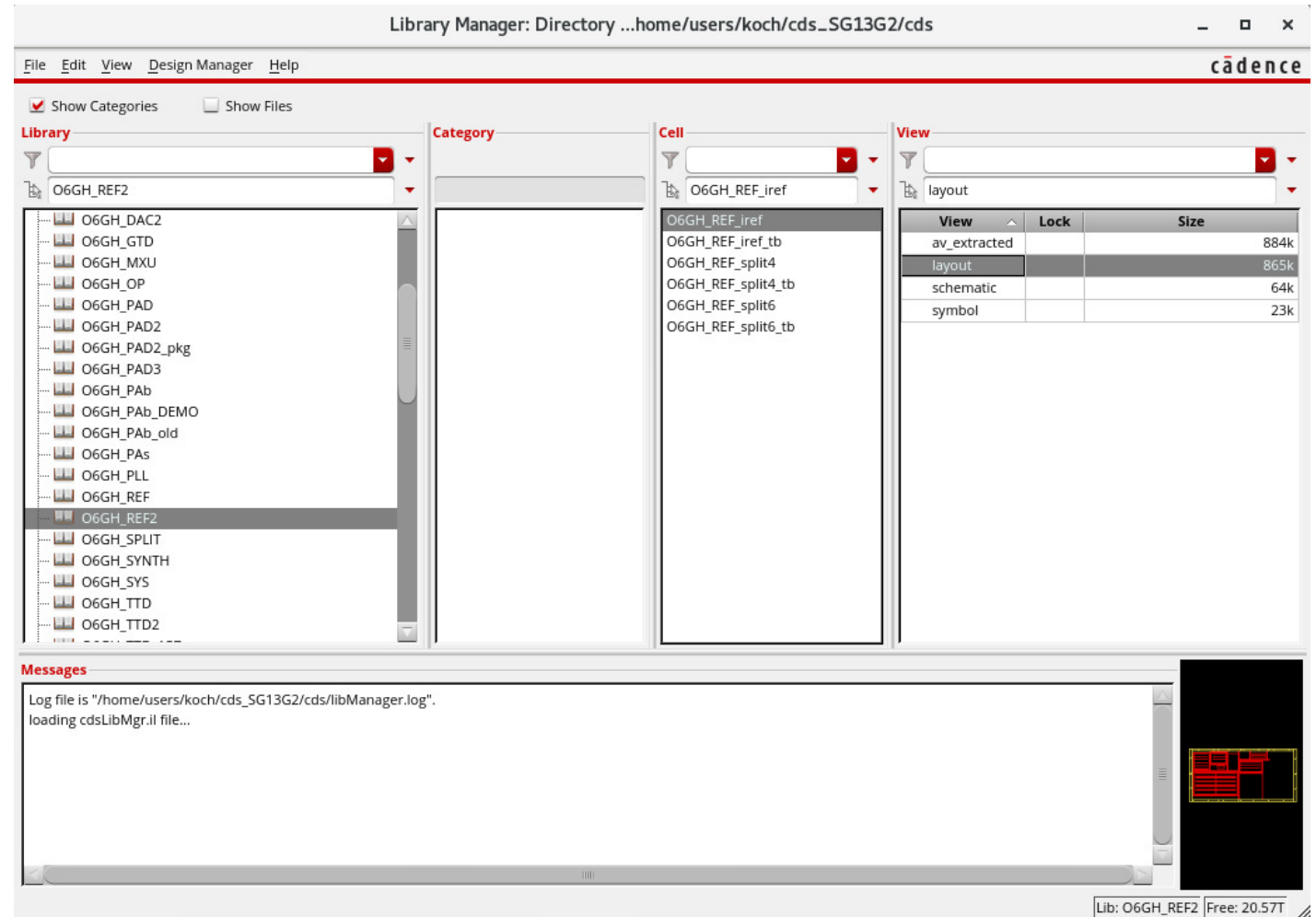
- Automated simulation of typical passive components



- Bandgap reference, current mirrors, DACs for biasing
 - Substrate PNPs, Mosfets
 - Monte Carlo Simulation
- Digital Designs
 - Synthesized from VHDL with Cadence Genus / Innovus with IHP stdcell library
 - Mixed signal simulation

OpenAccess Database

- Hierarchically stored data
- Cells / Directories with different views: schematic, layout, s-parameter, vhdl, ...



	Lab course	Thesis	Ph.D. students
Setup manual / Training videos	++	++	++
Simulation	sp, hb/pss with sp, transient	sp, hb/pss with sp, transient, pss for oscillator, (PVT)	sp, hb/pss with sp, transient, pss for oscillator, PVT
Simulation models	HBT, t-lines	HBT, t-lines, inductors, capacitors, Mosfets	HBT, t-lines, inductors, capacitors, Mosfets, transformers
Layout	Only visualization	Pcells, DRC, LVS, PEX	Pcells, DRC, LVS, PEX, Pads
Digital flow	0	0	++
EM simulation	0	+	++