PDKMaster and Standard cell generator for the open source IHP PDK

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IHP Workshop 2023

Background

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- Professional:
  - 24 years imec; last 7-8 years:
    - radiation hardened SRAM compiler development
    - customer support for radiation hardened libraries and analog/mixed-signal IP

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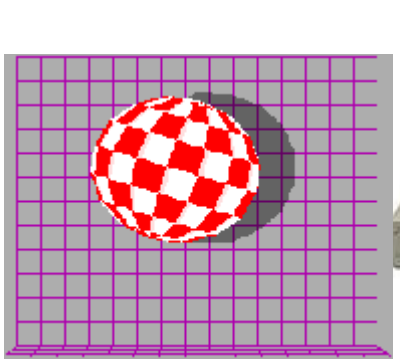
- Professional:
  - 24 year imec; last 7-8 years:
    - radiation hardened SRAM compiler development
    - customer support for radiation hardened libraries and analog/mixed-signal IP
- Hobby
  - (ex-) Amiga addict



  - Open source programmer
    (AROS; open source reimplementation of AmigaOS)
  - Python-lover

Background

- Personal motivation for my open source EDA and PDK involvement
  - Main purpose of open source is IMHO not about getting the source code but around building development communities around publicly shared source code.
  - Stagnated innovation for the EDA software
  - Each PDK is different making porting between them difficult; this has led to creation of PDKMaster
  - Not happy with VHDL/(System)Verilog;
    seems too much design by committee, not proper abstraction
    I am Amaranth user; other options Chisel, SpinalHDL, ...
  - Analog: design to spec vs. design for reuse + continuous improvement

Affiliations

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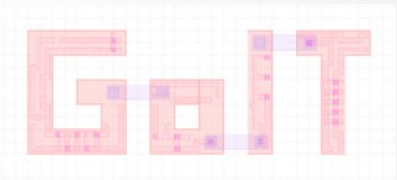
- Funding
  - NLnet project funds*:
    - NGI0 PET: Chips4Makers ASICS, LibreSOC & Analog/Mixed Signal Library
    - NGI Assure: LibreSOC Gigabit Router
  - GOIT European project*: https://goit-project.eu
- Founded own company FibraServi;
  chips4makers is an umbrella project from FibraServi
- Co-founded ChipFlow ltd.: https://chipflow.io



* Funded by the European Union. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or NLnet. Neither the European Union nor NLnet can be held responsible for them.

PDKMaster & co.

PDKMaster & co.

- Python based framework
  - Starting from the base; trying to develop a good API (takes time)
  - Using software engineering best practices for EDA
- Modules:
  - PDKMaster: framework for technology description, circuit and layout generation
  - c4m-flexcell: scalable standard cell library generation
  - c4m-flexio: scalable io cell library generation (→FSiC 2022)
  - c4m-flexmem: scalable memory compiler (→FSiC 2022)
  - scalable analog/mixed signal project (→ FSiC 2023)

PDKMaster & co.

- PDKs
  - currently maintained:
    - c4m-pdk-sky130
    - c4m-pdk-gf180mcu
    - c4m-pdk-ihpsg13g2
  - unmaintained
    - c4m-pdk-freepdk45
    - c4m-pdk-tsmc350
    - c4m-pdk-tsmc180

PDKMaster & co.

- Code demo in Visual Studio code

Status

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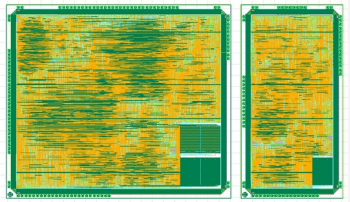
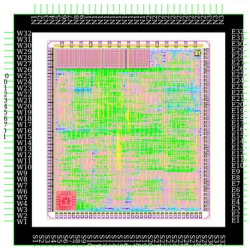
- Previous tape-outs:
  - Retro-µC: TSMC 0.35µm
    (https://chips4makers.io/blog/retro-mc-2021-test-tape-out.html;
    Chips4Makers project)
  - LibreSOC prototype: TSMC 0.18µm
    (https://libre-soc.org/180nm_Oct2020/;
    NLnet NGI0 PET)
  - Amaranth+Coriolis Test SoC: Sky130
    (https://platform.efabless.com/projects/691; ChipFlow project)





Status

- PDKMaster:
  - Technology definition: relative stable API
  - Circuit definition: relative stable API
  - Layout generation: very unstable API

Status

- PDK support:
  - Sky130
    - 1.3V std. cell libraries
    - IO cells
    - Few fixed size SRAM blocks (broken by latest version of std.cells)
  - gf180mcu
    - 3.3V and 5V std. cell libraries
  - Ihpsg13g2
    - 1.2 and 3.3 V std. cell libraries; GDS view only currently needs superficial N+ implant layer

Contact

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- Follow blog on https://chips4makers.io/blog or discuss possible use on gitter/matrix https://matrix.to/#/#Chips4Makers_community:gitter.im

Open questions

- Long term open source support for PDKs – PDKMaster included.
  Are users of the PDK also going to contribute to the development of the (base of the) PDK ?
  cfg. Heartbleed bug for OpenSSL: base library used by everyone but only parttime maintained by volunteers.
- Is fixing design flow making innovation more difficult?
  Is there one tool to rule them all ?