Rockchip
RK3576S
Datasheet

Revision History

Date	Revision	Description
2024-10-08	1.0	Initial release

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Warranty Disclaimer

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Chapter 1 Introduction

1.1 Overview

RK3576S is a low power, high performance processor for ARM-based PC and Edge Computing device, personal mobile internet device and other digital multimedia applications, and integrates quad-core Cortex-A72 and quad-core Cortex-A53 with separately NEON coprocessor.

RK3576S video decoder supports H.264, H.265, VP9, AV1 and AVS2 etc. up to 4K@60fps, and video encoder supports H.264 and H.265 up to 4K@30fps, high-quality JPEG encoder/decoder supports up to 4K@60fps.

Embedded 3D GPU makes RK3576S completely compatible with OpenGL ES 1.1, 2.0, and 3.2, OpenCL up to 2.0 and Vulkan 1.1. Dedicated 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

RK3576S introduces a new generation 16-Megapixel ISP (Image Signal Processor). It implements a lot of algorithm accelerators, such as HDR, 3A, CAC, 3DNR, 2DNR, Sharpening, Dehaze, Enhance, Debayer, Small Angle Lens-Distortion Correction and so on.

The build-in NPU supports INT4/INT8/INT16/FP16/BF16/TF32 hybrid operation. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RK3576S supports high-performance dual channel external memory interface (LPDDR4/LPDDR4X/LPDDR5) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

1.2 Features

1.2.1 Microprocessor

- Cortex A72 cluster
  - Quad Cortex A72 MPCore processor
  - 48kB L1 instruction cache and 32kB L1 data cache for each core
  - 1MB unified L2 cache
- Cortex A53 cluster
  - Quad Cortex A53 MPCore processor
  - 32kB L1 instruction cache and 32kB L1 data cache for each core
  - 512kB unified L2 cache

- TrustZone technology
- ARMv8 Cryptography Extensions
- Full implementation of the ARM architecture v8-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerating media and signal processing.
- Two isolated voltage domains to support DVFS, one is for A72 cluster and the other is for A53 cluster.
- Independent power domain for each CPU core system (CPU+Neon+FPU+L1 cache).

1.2.2 Memory Organization

- Internal on-chip memory
  - BootRom
    - Supports system boot from the following devices:
      - FSPI interface
      - eMMC interface
      - UFS interface
      - SD card interface
      - USB interface
    - Supports system code download by the following interface:
      - USB OTG interface
  - PMU_SRAM (32kB) is for low power application
  - SYS_SRAM (512kB) may be shared by any on-chip components
- External off-chip memory
  - Dynamic Memory interface
    - JEDEC standards LPDDR4/LPDDR4X-4266 and LPDDR5-4800.
    - Dual channels, each channel has 16bits data width.
    - Up to 2 ranks (chip select) for each channel.
    - Up to 16GB addressing space totally.
    - Low power mode including power-down and self-refresh with power-down.
  - eMMC interface
    - Compliance to JEDEC eMMC v5.1 specification
    - Compatible to eMMC 4.51 and earlier versions specification.
    - Supports HS400, HS200, DDR50 and legacy operating modes
    - Supports data bus width: 1-bit, 4-bit or 8-bit
  - SD/MMC interface
    - Compliance to SD v3.0, MMC v4.51
    - Supports 4-bit data bus
  - UFS interface
    - Compatible to UFS v2.0 specification

- Supports 2 data lanes
- Up to High-Speed Gear 3 (HS-G3B)

- Flexible Serial Flash Interface(FSPI)
  - Supports serial NOR, NAND, pSRAM, SRAM devices
  - Supports 1-bit, 2-bit, and 4-bit data width
  - Supports 2 chip selects for 1-bit, 2-bit, 4-bit FSPI

1.2.3 System Component

- MCU
  - Single core Cortex M0
  - 16kB unified I/D cache
  - Programmable Interrupt Controller
  - JTAG interface for debug
- CRU (clock & reset unit)
  - Supports 12 PLLs to generate all clocks totally
  - Supports one 24MHz oscillator as input
  - Supports clock gating control for individual components
  - Supports global soft-reset control for whole chip, also individual soft-reset for each component
- PMU (power management unit)
  - Supports multiple configurable work modes to save power consumption with different frequency or automatic clock gating control or power domain control
  - Supports many wakeup sources in different working state
  - Supports 7 separate voltage domains
  - Supports 30 separate power domains, which can be power up/down by software based on different application scenes
- Timer
  - Supports 12 secure timers with 64bits counter and interrupt-based operation
  - Supports 18 non-secure timers with 64bits counter and interrupt-based operation
  - Supports two operation modes: free-running and user-defined count for each timer
  - Supports timer work state checkable
- PWM
  - Supports 16 on-chip PWMs (PWM0_CH0~PWM0_CH1, PWM1_CH0~PWM1_CH5, PWM2_CH0~PWM2_CH7) with interrupt-based operation
  - Supports input capture mode
  - PWM0 and PWM2 support IR power key capture mode
  - Supports continuous mode and one-shot output mode
  - PWM1 supports generates waveform through lookup table
  - PMW2 supports IR transmission in NEC with full repeat, NEC with simple repeat,

TC9012 or SONY mode
    - PWM1 supports clock frequency meter
    - PWM1 supports clock counter
    - PWM1 and PWM2 support biphasic counter
    - Supports two-stage frequency division of working clock
- Watchdog
    - Supports 5 non-secure watchdog and 1 secure watchdog
    - 32-bit watchdog counter
    - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
    - WDT can perform two types of operations when timeout occurs:
        - Generate a system reset
        - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Interrupt Controller
    - Supports 4 PPI interrupt source and 480 SPI interrupt sources input from different components inside SoC
    - Supports 16 software-generated interrupts
    - Input interrupt level is fixed, high-level sensitive for SPI and low-level sensitive for PPI
    - Supports different interrupt priority for each interrupt source, and they are always software-programmable
- DMAC
    - Supports 3 DMA controllers for peripheral system
    - Supports Linked list DMA mode to complete scatter-gather transfer
    - Supports data transfer types including memory-to-memory, memory-to-peripherals and peripherals-to-memory
    - Each DMAC features:
        - Supports 8 channels
        - Supports 32 hardware request from peripherals
        - Supports 2 interrupt output
        - Supports TrustZone technology and programmable secure state
- Secure System
    - Supports one cipher engine
        - Supports 3 software interfaces including secure world, non-secure world and key-ladder world
        - Supports Link List item (LLI) DMA transfer
        - Supports symmetric and Hash algorithm lockstep error monitoring

- Supports symmetric algorithm anti side channel attack
- Supports Symmetrical algorithms
  - AES-128, AES-192, AES-256, DES, 3DES, SM4
  - ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode for AES and SM4
  - ECB/CBC/OFB/CFB mode for DES/TDES
- Hash algorithm
  - SHA-1, SHA-256/224, SHA-512/384, SHA-512MD5, SM3 with hardware padding
  - HMAC of SHA-1, SHA-256, SHA-512, MD5, SM3 with hardware padding
- Asymmetrical algorithms
  - RSA (up to 4096 bits), ECC (up to 256 bits), SM2
- Key-ladder(KL)
  - Supports obtaining the root key from OTP or RKRNG and deriving it
  - Supports write out root key or derived key to some specific modules
  - Number of stages can be configured

- Supports data scrambling for all DDR types
- Supports secure OTP
- Supports secure debug
- Supports secure DFT test
- Supports secure OS
- Except CPU, the other masters in the SoC can also support security and non-security mode by software-programmable
- Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
- System SRAM (share memory), part of space is addressed only in security mode
- External DDR space can be divided into 16 parts; each part can be software-programmable to be enabled by each master

- Mailbox
  - Supports one Mailbox with 14 channels in SoC to provide communication service between CPU and MCU
  - Supports independent interrupt in each Mailbox channel

1.2.4 Video Codec

- Video Decoder
  - Supports video decoder of H.264, H.265, VP9, AV1 and AVS2
  - Supports MMU
  - Supports multi-stream decoding in parallel

Decoder	Profile	Level	Resolution
H.264/AVC	Main10	5.2	up to 4K@60fps
H.265/HEVC	Main10	6.0	up to 4K@60fps
VP9	Profile 0/2	6.0	up to 4K@60fps
AVS2	Profile 0/2	8.2.120	up to 4K@60fps
AV1	Main10	6.0	up to 4K@60fps

  - H264 MVC is up to 4K@60fps

- Video Encoder

Encoder	Profile	Level	Resolution
H.264/AVC	High	5.2	up to 4K@30fps
H.265/HEVC	Main	5.1	Up to 4K@30fps

  - Supports multi-stream encoding

- JPEG Encoder
  - Supports Baseline (DCT sequential)
  - Supports image size is from 16x16 to 65520x65520
  - Supports MJPG up to 4K@60fps
  - Supports YUV400/ YUV420/YUV422/YUV444
- JPEG Decoder
  - Supports image size is from 48x48 to 65520x65520
  - Supports MJPG up to 4K@30fps
  - Supports YUV400/YUV411/YUV420/YUV422/YUV440/YUV444

1.2.5 Neural Process Unit

- Rockchip NPU engine:
  - 3 TOPS* for INT8
  - Supports dual core and support dual core co-work, or work independently
  - Supports INT4, INT8, INT16, FP16, BF16 and TF32 operation
  - Supports 1MB internal SRAM
  - Supports multi-task, multi-scenario in parallel
  - Supports deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, Android NN, etc.

  * Sparsity

1.2.6 Graphics Engine

- 3D Graphics Engine
  - ARM Mali G52 MC3 GPU
  - OpenGL ES 1.1, 2.0, and 3.2
  - Vulkan 1.1
  - OpenCL 2.0 Full Profile
  - AFBC (ARM Frame Buffer Compression)

- 2D Graphics Engine (RGA)
  - Rockchip RGA v2.5 engines with dual core
  - Max resolution: 8192x8192 source, 4096x4096 destination
  - Block transfer and Transparency mode
  - Color fill with gradient fill, and pattern fill
  - Alpha blending including global alpha, per pixel alpha and fading
  - Arbitrary non-integer scaling ratio from 1/16 to 16
  - 0, 90, 180, 270-degree rotation, x-mirror, y-mirror & rotation operation
- VDPP (Video & Display Post Process)
  - Deinterlace
    - Input data format: YUV420/YUV422, P/SP
    - Output data format: YUV420/YUV422, SP
    - Supports algorithms including I5O2, I5O1, I2O2, I1O1 and so on
    - Resolution is up to 1920x1080
  - Post Process
    - Input data format: YUV420SP
    - Output data format: YUV420/YUV444 SP
    - DMSR: De-Mosquito noise, De-Ringing effect and De-Shooting effect
    - ZME: Zoom Manage Engine (Video resize based Multi-Phase Algorithm)
    - DCI-HIST: Histogram of Dynamic Contrast improvement
    - SHARP: Sharpness
    - ES: Edge Smoothing

1.2.7 Video Input Interface

- Support 3 MIPI CSI-2 interfaces
  - Two 4 data lanes of D-PHY v1.2
    - Each interface may be configured as 2x2 data lanes port.
  - One 4 data lanes (or 3 data trios) of C/D-PHY
    - D-PHY is v2.0 which lane speed is 4.5Gbps
    - C-PHY is v1.1 which trio speed is 2.5Gsps
  - Each port supports 4 virtual channels
- DVP interface
  - 8/10/12/16-bit, up to 150MHz I/O frequency
  - BT.601/BT.656 and BT.1120 VI interface
  - Supports the polarity of pixel_clk, hsync, vsync configurable
  - Supports 2/4 mux byte interleave format for BT.656/BT.1120
  - Supports dual-edge sampling for BT.656/BT.1120

1.2.8 Image Signal Processor

- Video Capture (VICAP)

- Supports BT.601 RAW8/10/12 YUV422 8-bit input
- Supports BT.656 YUV422 8-bit progressive/interlaced input
- Supports BT.1120 YUV422 16-bit progressive/interlaced input
- Supports 2/4 mux byte interleave format for BT.656/BT.1120
- Supports dual-edge sampling for BT.656/BT.1120
- Supports receiving five groups of MIPI CSI interfaces, up to four IDs for each group
- Supports VC/DT configurable for each ID
- Supports MIPI CSI data formats: RAW8/10/12/14/16, RGB888, YUV422 8bit, YUV422 8bit interlaced, YUV420 8bit, Legacy YUV420 8bit
- Support three modes of MIPI CSI HDR: virtual channel mode, identification code mode, line counter mode
- Support window cropping
- Supports 8/16/32 times down-sampling for RAW data
- Supports RAW 2x2 binning
- Supports pixel extraction from 2x2 pattern
- Supports UV mean down sampling for YUV422
- Supports reducing frame rate
- Supports compact/non-compact output format for RAW data
- Supports NV16/NV12/YUV400/YUYV output format for YUV data
- Supports virtual stride when write to DDR
- Supports DMA burst gather 2/4/8
- Supports MMU
- Supports QOS(hurry/press)
- Supports sending RAW data directly to ISP
- Supports soft reset, auto-reset when DMA error
- Supports debug mode

- Image Signal Processor V3.9
  - One channel ISP, 16M pixels
  - VICAP/DMA input: raw8/raw10/raw12/raw16
  - RGB-IR sensor input
  - 3A: include AE/Histogram, AF, AWB statistics output
  - BLC: Black Level Correction
  - PDAF: Phase Detection Auto Focus
  - DPCC: Static/Dynamic defect pixel cluster correction
  - LSC: Lens shading correction
  - HDR: 2-Frame Merge into High-Dynamic Range
  - DRC/TMO: Dynamic Range Compression, Tone mapping in RGB field
    - Supports up to 120dB HDR with 20-bit data width

- EXPANDER: Sensor expander
- GIC: Green Imbalance Correction
- Debayer: Advanced Adaptive Demosaic with Chromatic Aberration Correction(CAC)
- CCM/CSM: Color correction matrix; RGB2YUV etc.
- Gamma: Gamma out correction
- Dehaze/Enhance: Automatic Dehaze and edge enhancement
- Bay3DNR: Advanced Temporal Noise reduce in RAW;
- YUVME: Noise Motion Estimate and Motion Compensation in YUV
- 2DNR: Advanced Spatial Noise reduce in YUV;
- Sharp: Picture Sharpening & Edge Enhance in YUV;
- CGC: Color Gamut Compression, YUV full range/limit range convert
- 3DLUT: 3D-Lut Color Palette for Customer;
- LDCH: Lens-distortion in the horizontal direction;
- LDCV: Lens-distortion in the vertical direction;
- Gain: Image local gain
- Output Scale*2: support scale down level;

1.2.9 VPSS

- VPSS
  - Offline DMA input:
    - Line RGB888/ARGB888/RGB565/YUV422/YUV420 SP 8bits
    - Tile4x4 YUV422/YUV420 8bits (Rotate 90/180/270)
    - RKFBCD64x4 YUV422/YUV420 8bits
  - Online ISP input
  - Both DMA and ISP input
  - Maximum input: 4672x3504 (width no more than 4672)
  - Minimum input: 32x32
  - MIRROR: Horizontal Mirror
  - CMSC: Cover or Mosaic in 8 areas
  - CROP: 4 channels Crop
  - Channel0 output:
    - SCALE: Poly-phase filter
    - ASPT_RATIO: aspect-ratio for image boundary extension
    - Either Line YUV422/YUV420 SP 8bits or Tile4x4 YUV422/YUV420 8bits
    - Flip: Vertical Flip
  - Channel1 output:
    - SCALE: Bilinear filter
    - ASPT_RATIO: aspect-ratio for image boundary extension
    - Either Line RGB888/ARGB888/RGB565/YUV422/YUV420 SP 8bits or Tile4x4

YUV422/YUV420 8bits
    - Flip: Vertical Flip
- Channel2 output:
    - SCALE: Bilinear filter, Maximum output: 1920x1080 (width no more than 1920)
    - ASPT_RATIO: aspect-ratio for image boundary extension
    - Line YUV422/YUV420 SP 8bits
    - Flip: Vertical Flip
- Channel3 output:
    - SCALE: Bilinear filter, Maximum output: 1920x1080 (width no more than 1920)
    - ASPT_RATIO: aspect-ratio for image boundary extension
    - Line YUV422/YUV420 SP 8bits
    - Flip: Vertical Flip
- Either channel0 or channel1 Tile4x4 output

1.2.10 Video Output Processor

- Video Port
    - Video Port0 supports up to 4K@120Hz with 10-bit data
- Data format
    - Raster:
        - ARGB8888/RGB8888/RGB565
        - YUV420/YUV422/YUV444, 8/10-bit
        - YUV444i
    - Tile 4x4
        - YUV420/YUV422/YUV444, 8/10-bit
    - FBCD 32x8 split (GPU)
        - RGB565/RGBA1010102/RGB888/RBGA8888
    - FBCD 64x4 (Video)
        - RGB565/RGBA1010102/RGB888/RBGA8888
        - YUV420/YUV422/YUV444, 8/10-bit
- Display Layer
    - Supports two type of display layers (Cluster and Esmart)
    - FBCD data is only supported in cluster layer
    - Layer split is only supported in cluster layer
    - Multi-region is only supported in Esmart layer
    - Supports Data swap, replication, offset, virtual display
    - Supports scaling down/up with the ratio 1/4~8, subject to VOP performance in the conditions of high resolution and high frame rate. For 4k@120, we recommend that you use RGA for scaling.
    - Supports CSC (Color Space Convert) for BT601/BT709/BT2020

- Cluster layer
  - Supports 2 cluster layers
  - Supports resolution is up to 4kx2k
  - Supports FBC 32x8 and FBC 64x4
  - Supports rotation
- Esmart layer
  - Supports 4 Esmart layers
  - Supports resolution up to 4k for 2 layers and 2k for the other 2 layers
  - Supports 4 regions in each layer

- Overlay
  - Supports Layer position exchange
  - Supports transparency color key and 8BPP alpha blending
  - Supports per-pixel alpha, pre-multiplied alpha and global alpha
  - Supports RGB or YUV domain overlay
- Post Process
  - Supports HDR10/HLG/HDR Vivid
  - Supports Post scale
  - Supports Dither down
  - Supports CSC, color domain and color range convert.
  - Supports Gamma/3D-LUT
  - Supports ACM, auto color management
  - Supports DCI, dynamic contrast improvement
  - Supports SHARPNESS
- Write Back
  - Output data format: XRGB8888/RGB888/RGB565/YUV420
  - Max resolution: 1920x1080
  - Support virtual stride
  - Supports automatic write back and one frame write back model
  - Supports horizontal scale

1.2.11 Display interface

- HDMI/eDP TX interface
  - One HDMI/eDP TX combo interface
  - HDMI interface
    - HDMI v2.1
    - Supports up to 4K@120Hz
    - Output data format: RGB/YUV444/YUV422/YUV420 8/10-bit
    - Supports CEC (Consumer Electronic Control) and ARC (Audio Return Channel)
    - HDCP v2.3 and HDCP v1.4

- eDP interface
  - eDP v1.3 and compliant with DisplayPort v1.2
  - Main link containing 4 physical lanes
  - Each lane supports RBR(1.62Gbps), HBR(2.7Gbps) and HBR2(5.4Gbps)
  - Supports up to 4K@60Hz
  - Output data format: RGB/YUV444/YUV422 8/10-bit
  - Supports HDCP v1.3
  - Supports PSR (Panel Self Refresh)
  - Supports I2S (up to 8 channels) and S/PDIF audio interface
  - Supports AUX and reading of the display EDID
- DisplayPort TX and USB combo interface
  - Supports one USBDP combo PHY
    - Supports USB3.2 Gen1x1 and DisplayPort v1.4
    - Supports 4 transmission data lanes
    - Supports USB Type-C AltMode
  - DisplayPort TX controller
    - DisplayPort v1.4
    - Supports 1/2/4 lanes with lane speed including 1.62、2.7、5.4 and 8.1Gbps
    - Supports up to 4K@120Hz
    - Output data format: RGB/YUV444/YUV422/YUV420 8/10-bit
    - Supports Multi-Stream Transport (MST) with 3 displays
    - Supports DP AltMode on USB Type-C
    - Supports HDCP v2.3 and HDCP v1.3
  - USB controller
    - Supports USB3.2 Gen1x1
    - Supports Dual-Role Device (DRD)
    - Supports xHCI Host with up to 64 devices
- MIPI DSI-2 TX interface
  - One MIPI DSI-2 v1.1 interface with D-PHY v2.0 or C-PHY v1.1
  - Supports 4 data lanes on D-PHY with up to 2.5Gbps per lane
  - Supports 3 data trios on C-PHY with 1.7Gsps per trio
  - Supports RGB (up to 10bit) data format

1.2.12 Serial Audio Interface (SAI)

- Supports five SAI interfaces
  - SAI 0/1 support 4 TX lanes and 4 RX lanes
  - SAI 2/3/4 support 1 TX lane and 1 RX lane
  - Supports I2S/TDM/PCM mode
  - Supports 3 I2S formats (normal, left-justified, right-justified)

- Supports master and slave work mode, software configurable
- Supports 4 PCM formats (early, late1, late2, late3)
- Supports TDM normal, 1/2 cycle left shift, 1 cycle left shift, 2 cycle left shift, right shift mode serial audio data transfer
- Supports sample rate is up to 192KHz
- Supports audio resolution is from 16bits to 32bits

- SPDIF TX
  - Two SPDIF TX ports
  - Supports two 16-bit audio data store together in one 32-bit wide location
  - Supports bi-phase format stereo audio data output
  - Supports 16 to 31-bit audio data left or right justified in 32-bit wide sample data buffer
  - Supports 16, 20, 24 bits audio data transfer in linear PCM mode
  - Supports non-linear PCM transfer
- SPDIF RX
  - Two SPDIF RX ports
  - Supports one internal 30-bit wide and 32-location deep FIFO for receiving audio data
  - Supports combined interrupt output
  - Supports DMA handshaking interface and configurable DMA water level
  - Supports liner PCM(IEC60958) and non-liner PCM(IEC61937)
  - Supports 16~24 bits audio sample length for liner PCM application
  - Supports 16 bits audio sample length for non-liner PCM application
  - Supports up to 384kHz sample rate with the corresponding reference clock equal to 384KHz*64*2*10, that is 491.52MHz
  - Supports the frequency of reference clock is at least 10 times the frequency of the bi-phase encoding clock, but not more than 256 times
  - Supports recovering clock and audio data from input bit-stream
- PDM0/PDM1
  - Supports up to 8 channels
  - Supports resolution is from 16bits to 24bits
  - Supports sample rate is up to 192KHz
  - Supports PDM master receive mode
  - Supports gain control
- ASRC
  - Supports dual 2-channel ASRC and dual 4-channel ASRC
  - Supports fixed length conversion mode and real time conversion mode
  - Supports asynchronous sample rate clock for real time conversion mode

- Digital Audio Codec
  - Support 2 channels digital DAC
  - Support I2S/PCM interface, master and slave mode
  - Support 16-bit sample resolution
  - Support three modes of mixing for every digital DAC channel
  - Support volume control

1.2.13 Connectivity

- SDIO interface
  - SDIO v3.0
  - 4-bit data bus widths
- Combo high speed interface
  - Supports one PCIe2.1 interface with one data lane
    - Supports PCIe v2.1
    - Supports Root Complex(RC) only
    - Supports up to 5GT/s data rate
- SPI interface
  - 5 SPI ports
  - Supports two chip-select in each interface
  - Supports serial-master and serial-slave mode, software-configurable
- I2C interface
  - 10 I2C ports in Master mode
  - Supports 7-bit and 10-bit address mode
  - Software programmable clock frequency
  - Supports data rate is up to 100kbps in the Standard-mode and si up to 400kbps in the Fast-mode
- I3C interface
  - Two I3C master ports
  - Compliance with I2C
  - Supports SDR mode
  - Supports In-Band interrupt（IBI）
  - Supports hot-join onto I3C bus
  - Supports dynamical and static slave address assigned
  - Supports up to 10 devices
  - Supports error detection (CE0~CE2)
- UART interface
  - 12 UART ports
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Supports 5bit, 6bit, 7bit, 8bit serial data transmit or receive

- Standard asynchronous communication bits such as start, stop and parity
- Supports different input clock for UART operation to get up to 8Mbps baud rate
- UART1~UART11 support auto flow control mode
- UART1-UART11 support RS485 function

- FlexBus interface
  - Supports built-in DMA and ping-pong operation for allocating two address
  - Supports transmission and receiving mode
  - Supports clock port two modes, free running and following data mode
  - Supports configurable four possible combinations for the clock polarity and phase
  - Supports single mode and continuous mode

1.2.14 Others

- Multiple group of GPIO
  - All of GPIOs can be used to generate interrupt
  - Supports level trigger and edge trigger interrupt
  - Supports configurable polarity of level trigger interrupt
  - Supports configurable rising edge, falling edge and both edge trigger interrupt
  - Supports configurable pull direction (a weak pull-up and a weak pull-down)
  - Supports configurable drive strength
- Temperature Sensor (TS-ADC)
  - Supports User-Defined Mode and Automatic Mode
  - In User-Defined Mode, start_of_conversion can be controlled completely by software, and also can be generated by hardware.
  - In Automatic Mode, the temperature of alarm (high/low temperature) interrupt can be configurable
  - In Automatic Mode, the temperature of system reset can be configurable
  - Supports 6-channel TS-ADC with the temperature criteria can be configurable
  - -40~125°C temperature range and 1°C temperature resolution
- Successive approximation ADC (SARADC)
  - Supports 12-bit resolution
  - Supports up to 1MS/s sampling rate
  - Supports 8 single-ended input channels
- OTP
  - Supports 16-kbit space and higher 4kbit address space is non-secure part.
  - Supports read and program word mask in secure model
  - Supports maximum 32 bit OTP program operation
  - Supports maximum 16 word OTP read operation
  - Program and Read state can be read

- Program fail address record

- Package Type
  - FCCSP698L (body: 16.1mm x 17.2mm; ball size: 0.30mm; ball pitch: 0.55mm&0.60mm&0.65mm mixed)

1.3 Block Diagram

The following figure shows the basic block diagram.

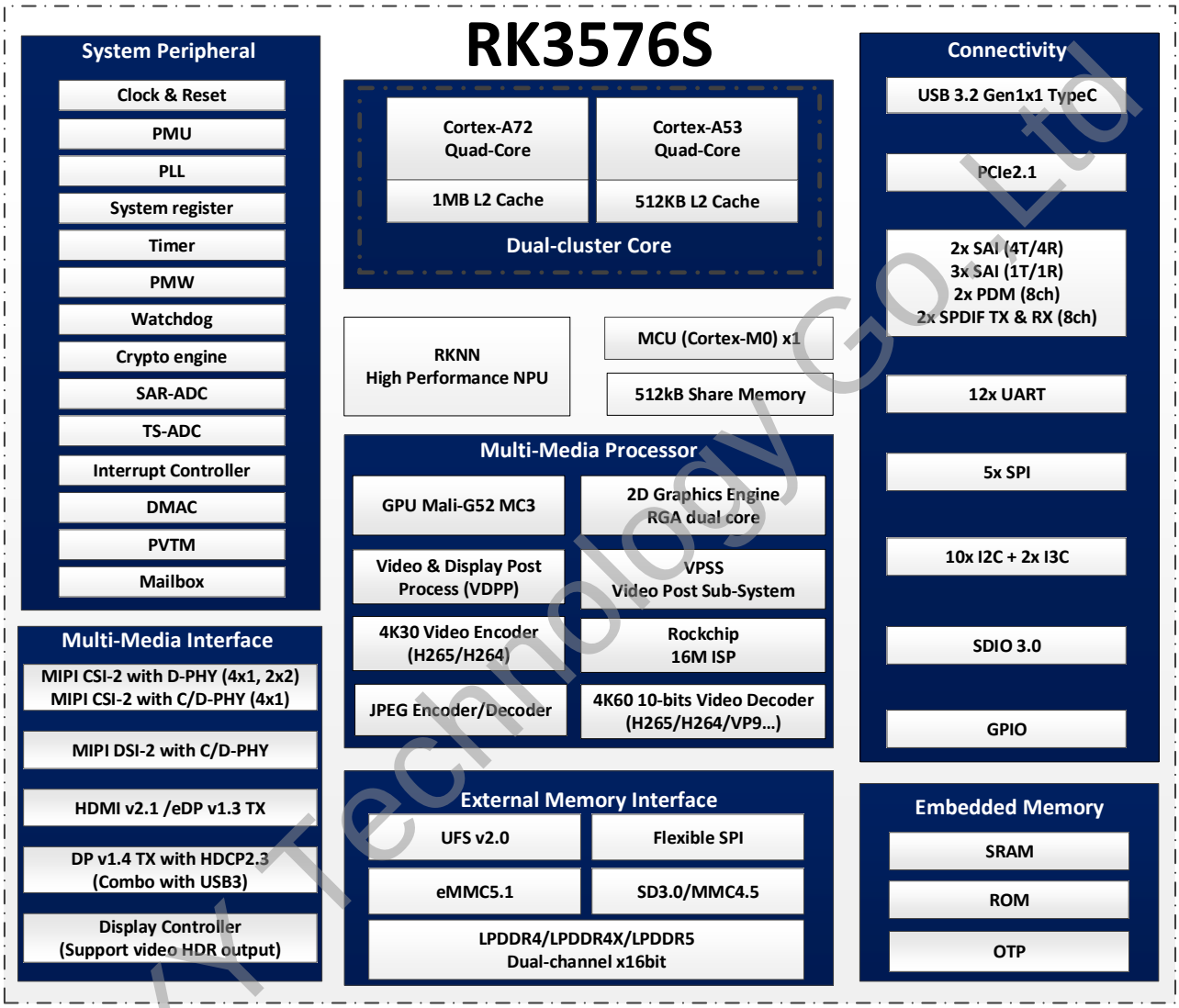

Fig.1-1 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package QTY	Device Feature
RK3576S	RoHS	FCCSP698L	840PCS	Application processor

2.2 Top Marking

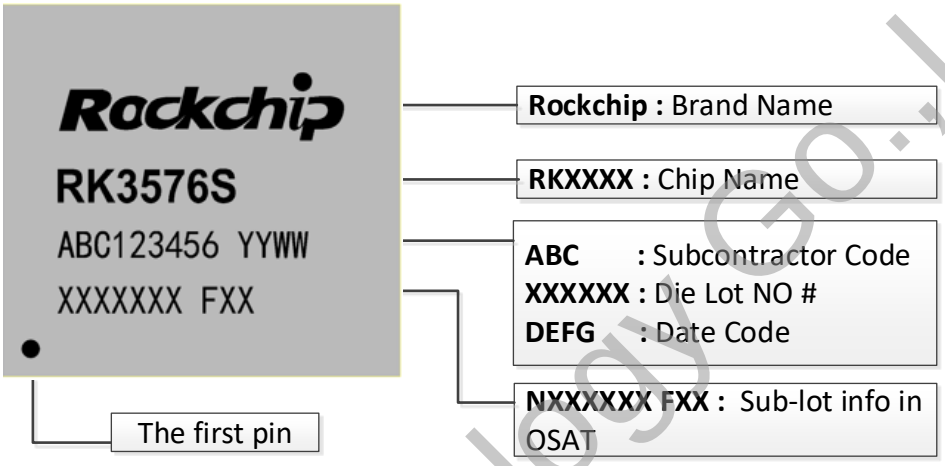

Fig.2-1 Package Definition

2.3 Package Dimension

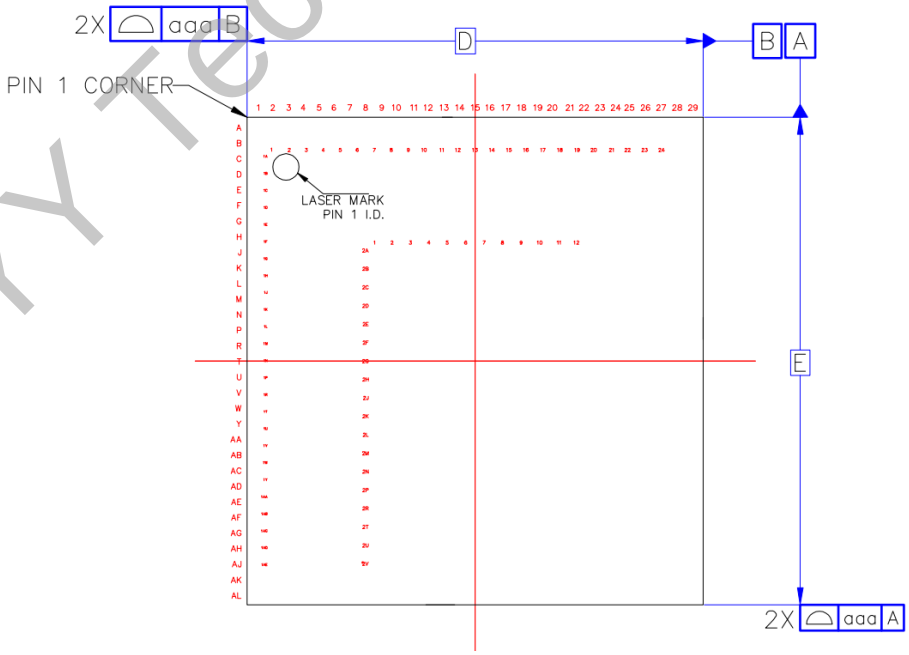

Fig.2-2 Package Top View

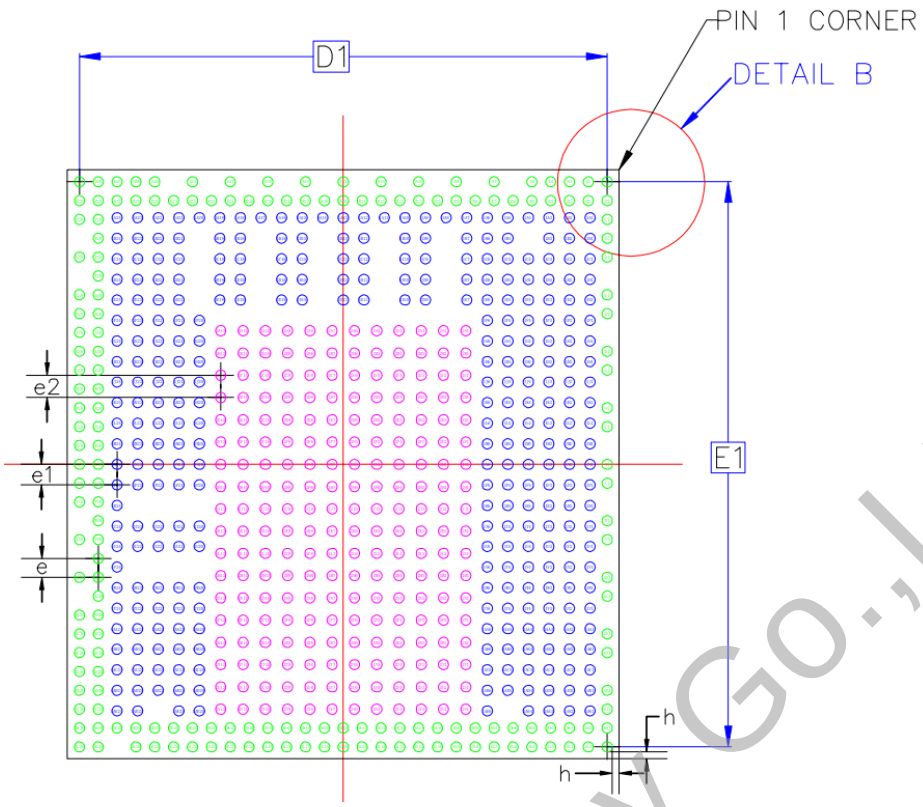

Fig.2-3 Package Bottom View

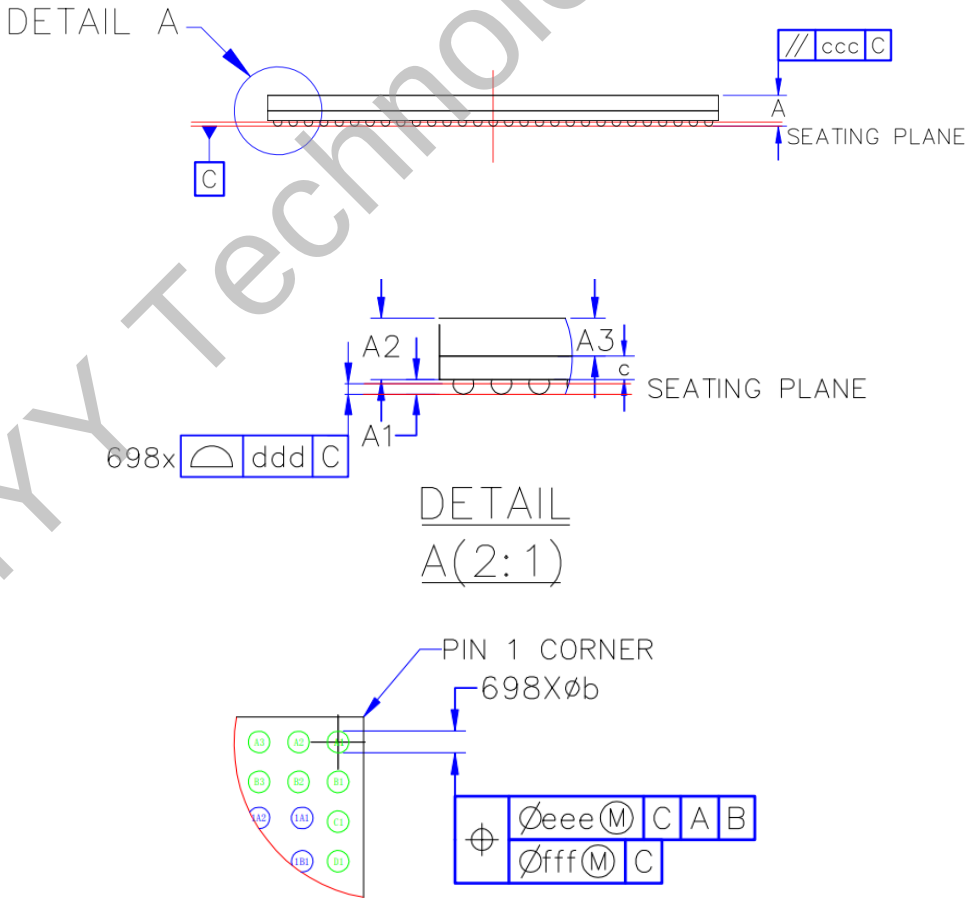

Fig.2-4 Package Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.92	1.00	1.081
A1	0.16	0.215	0.27
A2	0.73	0.79	0.85
c	0.30	0.34	0.38
A3	0.45 BASIC		
E	17.10	17.20	17.30
E1	16.50 BASIC		
D	16.00	16.10	16.20
D1	15.40 BASIC		
e	0.55 BASIC		
e1	0.60 BASIC		
e2	0.65 BASIC		
b	0.25	0.30	0.35
h	0.20REF		
aaa	0.15		
ccc	0.20		
ddd	0.08		
eee	0.15		
fff	0.08		

Fig.2-5 Package Dimension

2.4 MSL Information

Moisture sensitivity Level：3

2.5 Lead Finish/Ball Material Information

Lead finish/ball material：SnAgCu

2.6 Pin Number List

Table 2-1 Pin Number Order Information

Pin Name	Pin	Pin Name	Pin
VSS_0	A1	LP4_A1_A/LP4X_A1_A/LP5_A1_A	1N1
LP4_DQ11_B/LP4X_DQ11_B/LP5_DQ11_B	A2	VSS_59	1N2
LP4_DQS1P_B/LP4X_DQS1P_B/LP5_RDQS1P_B	A3	LP4_CKE0_A/LP4X_CKE0_A/LP5_CSN0_A	1N3
VSS_1	A4	VSS_60	1N4
LP4_DQ6_B/LP4X_DQ6_B/LP5_DQ6_B	A5	LP4_CKE1_A/LP4X_CKE1_A/LP5_CSN1_A	1N5
SAI1_SDO0_M0/SAI4_SDI_M0/SPI3_CLK_M2/PWM2_CH6_M0/GPIO4_A7_d	A7	VSS_61	1N6
VO_LCDC_D22/PDM1_SDI3_M2/FLEXBUS0_D7/UART1_RTSN_M2/SPI2_CSN1_M2/PWM1_CH1_M3/GPIO3_A5_d	A9	AVSS1_20	1N20
VO_LCDC_D16/PDM1_SDI0_M2/FLEXBUS0_D2/UART9_TX_M1/I2C8_SCL_M3/GPIO3_B3_d	A11	AVSS1_21	1N21
VO_LCDC_D17/PDM1_SDI1_M2/FLEXBUS0_D3/UART9_RX_M1/I2C8_SDA_M3/GPIO3_B2_d	A13	PCIE0_REFCLKP	1N22
VI_CIF_D2/SAI2_LRCK_M1/PDM1_SDI3_M0/UART11_RTSN_M1/SPI1_MISO_M1/PWM0_CH0_M2/GPIO2_C3_d	A15	PCIE0_REFCLKN	1N23
VI_CIF_D5/PDM1_SDI1_M0/UART9_RX_M0/PWM1_CH0_M2/GPIO2_C0_d	A17	AVSS1_22	1N24
VI_CIF_D9/SDMMC1_PWREN_M1/SAI0_SDI3_M0/PDM0_SDI0_M3/UART7_CTSN_M0/SPI4_MOSI_M3/GPIO2_B4_d	A19	LP4_DQ2_A/LP4X_DQ2_A/LP5_DQ2_A	1P1
VI_CIF_D7/SAI0_SCLK_M0/UART7_TX_M0/UART8_RTSN_M1/I2C8_SCL_M2/GPIO2_B6_d	A21	VSS_62	1P2
SDMMC0_D2/FSPI1_D2_M0/DSM_AUD_RP_M0/SAI3_LRCK_M3/JTAG_TCK_M0/UART5_RTSN_M2/SPI0_CSN1_M1/I3C1_SCL_M1/GPIO2_A2_d	A23	VSS_63	1P3
SARADC_IN0_BOOT	A25	VSS_64	1P4
FSPI1_D2_M1/PDM0_SDI0_M2/UART2_TX_M0/I2C8_SCL_M1/GPIO1_C6_d	A26	LP4_A5_A/LP4X_A5_A/LP5_A5_A	1P5
SDMMC1_D3_M0/SAI3_SDI_M1/UART3_RTSN_M2/SPI1_CSN0_M0/GPIO1_B7_d	A27	VSS_65	1P6
SDMMC1_D0_M0/SAI3_SCLK_M1/I2C9_SDA_M1/SPI1_CLK_M0/PWM1_CH0_M1/GPIO1_B4_d	A28	VSS_66	1P20
VSS_2	A29	VSS_67	1P21
LP4_DQ9_B/LP4X_DQ9_B/LP5_DQ9_B	B1	VSS_68	1P22
LP4_DQ10_B/LP4X_DQ10_B/LP5_DQ10_B	B2	SPI2_MISO_M0/I2C0_SDA_M0/GPIO0_B1_z	1P23
LP4_DQS1N_B/LP4X_DQS1N_B/LP5_RDQS1N_B	B3	VSS_69	1P24
LP4_DMI0_B/LP4X_DMI0_B/LP5_DMI0_B	B4	VSS_70	1R1
VSS_3	B5	VSS_71	1R2
SAI1_SDO3_M0/SAI1_SDI1_M0/PDM1_SDI1_M1/FLEXBUS1_D15_M1/SPI4_MISO_M2/MIPI_TE_M0/GPIO4_B2_d	B6	LP4_A2_A/LP4X_A2_A/LP5_A2_A	1R3
SAI1_SDO2_M0/SAI1_SDI2_M0/PDM1_SDI2_M1/FLEXBUS1_D14_M1/SPI4_MOSI_M2/UART5_RX_M1/UART6_CTSN_M0/UART2_CTSN_M1/GPIO4_B1_d	B7	LP4_CSN0_A/LP4X_CSN0_A	1R4
SPDIF_RX0_M0/FLEXBUS0_CSN_M4/UART2_RX_M1/I2C3_SDA_M0/GPIO4_B4_d	B8	LP5_A6_A	1R5
VO_LCDC_D9/SAI2_SCLK_M2/FLEXBUS0_D9/UART11_RTSN_M0/SPI4_MISO_M1/I2C9_SCL_M3/PWM2_CH0_M3/GPIO3_C2_d	B9	ZQ_A	1R6

Pin Name	Pin	Pin Name	Pin
VO_LCDC_D15/SPDIF_RX1_M0/FLEXBUS0_D1/UART9_RTSN_M1/PWM1_CH4_M3/GPIO3_B4_d	B10	TSADC_CTRL_M0/TSADC_CTRL_ORG/GPIO0_A1_z	1R24
VO_LCDC_D13/FLEXBUS0_CLK/SPI3_CSN0_M1/PWM0_CH1_M3/GPIO3_B6_d	B11	LP4_DQ1_A/LP4X_DQ1_A/LP5_DQ1_A	1T1
VO_LCDC_D0/SAI2_SDO_M2/FLEXBUS1_D2/UART2_CTSN_M2/I3C1_SCL_M2/PWM2_CH5_M3/GPIO3_D3_d	B12	LP4_A3_A/LP4X_A3_A/LP5_A3_A	1T2
VO_LCDC_D20/PDM1_CLK1_M2/FLEXBUS0_D5/UART1_TX_M2/UART10_RTSN_M0/GPIO3_A7_d	B13	VSS_72	1T3
VO_LCDC_D19/SAI4_MCLK_M1/FLEXBUS0_D8/UART10_RX_M0/SPI2_MOSI_M2/PWM0_CH0_M3/GPIO3_B0_d	B14	LP4_CSN1_A/LP4X_CSN1_A	1T4
SAI4_LRCK_M3/UART4_RTSN_M0/I2C5_SDA_M2/PWM0_CH1_M2/GPIO2_C7_d	B15	VSS_73	1T5
SAI4_SDI_M3/UART4_TX_M0/I2C6_SCL_M2/PWM2_CH0_M2/GPIO2_D0_d	B16	VSS_74	1T6
CAM_CLK0_OUT_M1/SAI4_MCLK_M3/UART6_TX_M1/I3C1_SCL_M0/PWM2_CH2_M2/GPIO2_D2_d	B17	VSS_75	1T20
UART6_RX_M1/I3C1_SDA_M0/PWM2_CH3_M2/GPIO2_D3_d	B18	PMIC_INT/GPIO0_A6_u	1T21
VI_CIF_D13/SDMMC1_D2_M1/SAI0_SDI0_M0/PDM0_SDI3_M3/UART1_TX_M1/GPIO2_B0_d	B19	SPI2_CLK_M0/I2C1_SCL_M0/GPIO0_B2_z	1T22
VI_CIF_D14/SDMMC1_D1_M1/SAI0_SDO1_M0/UART8_RX_M1/I2C4_SDA_M2/GPIO2_A7_d	B20	SPI2_MOSI_M0/I2C1_SDA_M0/GPIO0_B3_z	1T23
VI_CIF_D6/SAI0_LRCK_M0/UART7_RX_M0/UART8_CTSN_M1/I2C8_SDA_M2/GPIO2_B7_d	B21	PWR_CTRL2/GPIO0_A4_d	1T24
VI_CIF_D15/SDMMC1_D0_M1/SAI0_SDO0_M0/UART8_TX_M1/SPI4_CSN1_M3/I2C4_SCL_M2/GPIO2_A6_d	B22	LP4_DQS0P_A/LP4X_DQS0P_A/LP5_RDQS0P_A	1U1
SDMMC0_D3/FSPI1_D3_M0/DSM_AUD_RN_M0/SAI3_SDI_M3/JTAG_TMS_M0/UART5_CTSN_M2/I3C1_SDA_M1/GPIO2_A3_d	B23	VSS_76	1U2
SDMMC0_D0/FSPI1_D0_M0/DSM_AUD_LP_M0/UART0_RX_M1/UART7_RX_M2/I2C8_SCL_M0/SPI0_MOSI_M1/PWM2_CH2_M0/GPIO2_A0_d	B24	VSS_77	1U3
SDMMC0_D1/FSPI1_D1_M0/DSM_AUD_LN_M0/SAI3_MCLK_M3/UART0_TX_M1/UART7_TX_M2/I2C8_SDA_M0/SPI0_MISO_M1/PWM2_CH3_M0/GPIO2_A1_d	B25	VSS_78	1U4
SDMMC1_CMD_M0/PDM0_SDI2_M2/UART3_TX_M2/SPI1_CSN1_M0/PWM0_CH0_M1/GPIO1_C0_d	B26	LP4_RESET/LP4X_RESET/LP5_RESET	1U5
SDMMC1_D1_M0/SAI3_LRCK_M1/I2C9_SCL_M1/SPI1_MOSI_M0/PWM1_CH1_M1/GPIO1_B5_d	B27	VSS_79	1U6
FSPI1_D1_M1/UART4_RX_M1/UART2_CTSN_M0/SPI2_MISO_M1/GPIO1_C5_d	B28	PMUIO1_VCC	1U20
SDMMC1_PWREN_M0/FSPI1_RSTN_M1/FSPI1_CSN1_M1/UART4_RTSN_M1/I2C6_SCL_M1/SPI2_CSN1_M1/PWM1_CH2_M1/GPIO1_C2_u	B29	SDMMC0_DETN/SPI2_CSN1_M0/GPIO0_A7_u	1U21
VSS_4	C1	AUPLL_CLK_IN_M1/SPI2_CSN0_M0/I2C0_SCL_M0/GPIO0_B0_z	1U22
SAI2_SDI_M0/I3C0_SDA_M1/PWM1_CH4_M1/GPIO1_D3_d	C28	CLK_32K_IN/CLK0_32K_OUT/I2C6_SCL_M0/GPIO0_A2_d	1U23
SAI2_SDO_M0/UART10_TX_M1/GPIO1_D0_d	C29	UART0_TX_M0/JTAG_TCK_M1/GPIO0_D4_u	1U24
LP4_DQ15_B/LP4X_DQ15_B/LP5_DQ15_B	D1	LP4_DMI0_A/LP4X_DMI0_A/LP5_DMI0_A	1V1
EMMC_D6/SAI3_LRCK_M0/PDM0_CLK1_M1/SPI0_MISO_M2/I2C9_SDA_M0/GPIO1_A6_u	D28	VSS_80	1V2

Pin Name	Pin	Pin Name	Pin
LP4_DQ14_B/LP4X_DQ14_B/LP5_DQ14_B	E1	LP4_DQ4_A/LP4X_DQ4_A/LP5_DQ4_A	1V3
EMMC_D0/FSPI0_D0/SAI0_SCLK_M2/UART7_RTSN_M1/I2C2_SCL_M1/GPIO1_A0_u	E28	LP5_WCK0N_A	1V4
EMMC_D1/FSPI0_D1/SAI0_LRCK_M2/UART7_CTSN_M1/I2C2_SDA_M1/GPIO1_A1_u	E29	LP5_WCK0P_A	1V5
EMMC_D3/FSPI0_D3/SAI0_SDO2_M2/SAI0_SDI2_M2/PDM0_SDI1_M1/UART7_RX_M1/UART6_CTSN_M2/GPIO1_A3_u	F28	VSS_81	1V6
LP4_DQ7_B/LP4X_DQ7_B/LP5_DQ7_B	G1	I2C0_SDA_M1/UART8_RX_M2/I3C0_SDA_M0/GPIO0_C2_d	1V24
EMMC_D5/SAI3_SCLK_M0/PDM0_SDI2_M1/SPI0_MOSI_M2/I2C9_SCL_M0/GPIO1_A5_u	G28	VSS_82	1W1
AVSS1_0	G29	LP4_DQ13_A/LP4X_DQ13_A/LP5_DQ13_A	1W2
LP4_DQS0P_B/LP4X_DQS0P_B/LP5_RDQS0P_B	H1	VSS_83	1W3
MIPI_DPHY_CSI3_RX_D0P	H28	LP4_DQ5_A/LP4X_DQ5_A/LP5_DQ5_A	1W4
MIPI_DPHY_CSI3_RX_D0N	H29	VSS_84	1W5
MIPI_DPHY_CSI3_RX_D1P	J28	VSS_85	1W6
MIPI_DPHY_CSI3_RX_D1N	J29	MIPI_DPHY_CSI1/2_RX_AVDD1V8	1W20
LP4_DQ3_B/LP4X_DQ3_B/LP5_DQ3_B	K1	PDM0_CLK1_M0/HDMI_TX_CEC_M1/SPI0_CSN1_M0/PWM0_CH1_M0/GPIO0_C3_d	1W21
MIPI_DPHY_CSI3_RX_D2P/MIPI_DPHY_CSI4_RX_D0P	K28	SAI0_MCLK_M1/PDM0_CLK0_M0/UART10_TX_M2/PWM0_CH0_M0/GPIO0_C4_d	1W22
MIPI_DPHY_CSI3_RX_D2N/MIPI_DPHY_CSI4_RX_D0N	K29	SAI0_SDI0_M1/PDM0_SDI0_M0/SPI0_MOSI_M0/GPIO0_D0_d	1W23
LP4_A0_B/LP4X_A0_B/LP5_A0_B	L1	I2C2_SCL_M0/UART1_TX_M0/NPU_AVS/PWM1_CH4_M0/GPIO0_B7_d	1W24
MIPI_DPHY_CSI3_RX_D3P/MIPI_DPHY_CSI4_RX_D1P	L28	LP4_DQ12_A/LP4X_DQ12_A/LP5_DQ12_A	1Y1
MIPI_DPHY_CSI3_RX_D3N/MIPI_DPHY_CSI4_RX_D1N	L29	VSS_86	1Y2
N/A	M28	VSS_87	1Y3
N/A	M29	VSS_88	1Y4
LP4_CLKN_B/LP4X_CLKN_B/LP5_CLKN_B	N1	VSS_89	1Y5
N/A	N28	VSS_90	1Y6
N/A	N29	AVSS_9	1Y20
LP4_CLKN_A/LP4X_CLKN_A/LP5_CLKN_A	P1	SAI0_SCLK_M1/I2C3_SCL_M1/SPI0_CSN0_M0/GPIO0_C6_d	1Y21
PCIE0_TXN	P28	SAI0_SDI2_M1/SAI0_SDO2_M1/PDM0_SDI2_M0/I2C4_SCL_M0/CPUBIG_AVS/PWM1_CH5_M0/UART1_CTSN_M0/GPIO0_D2_d	1Y22
PCIE0_TXP	P29	SAI0_LRCK_M1/I2C3_SDA_M1/SPI0_CLK_M0/GPIO0_C7_d	1Y23
PCIE0_RXP	R28	SDMMC0_PWREN/SDMMC1_DETN_M2/HDMI_TX_HPDIN_M1/EDP_TX_HPDIN_M1/PWM1_CH2_M0/GPIO0_B6_d	1Y24
PCIE0_RXN	R29	LP4_DQ15_A/LP4X_DQ15_A/LP5_DQ15_A	1AA1
LP4_A0_A/LP4X_A0_A/LP5_A0_A	T1	VSS_91	1AA2
AVSS1_1	T28	LP4_DQ14_A/LP4X_DQ14_A/LP5_DQ14_A	1AA3
AVSS1_2	T29	VSS_92	1AA4
LP4_DQ3_A/LP4X_DQ3_A/LP5_DQ3_A	U1	LP5_WCK1N_A	1AA5
OSC_XIN	U28	LP5_WCK1P_A	1AA6
OSC_XOUT	U29	HDMI_TX_REXT/EDP_TX_REXT	1AA20
VSS_5	V28	VSS_93	1AA21

Pin Name	Pin	Pin Name	Pin
REF_CLK0_OUT/AUPLL_CLK_IN_M0/GPIO0_A0_d	V29	SAI0_SDO0_M1/DP_HPDIN_M1/UART10_RX_M2/I3C0_SDA_PU_M0/GPIO0_C5_d	1AA22
LP4_DQ0_A/LP4X_DQ0_A/LP5_DQ0_A	W1	SAI0_SDI3_M1/SAI0_SDO1_M1/PDM0_SDI3_M0/I2C4_SDA_M0/GPU_AVS/PWM2_CH0_M0/UART1_RTSN_M0/GPIO0_D3_d	1AA23
NPOR	W28	VSS_94	1AA24
LP4_DQS0N_A/LP4X_DQS0N_A/LP5_RDQS0N_A	Y1	LP4_DQ9_A/LP4X_DQ9_A/LP5_DQ9_A	1AB1
PWR_CTRL1/TSADC_CTRL_M1/GPIO0_A3_d	Y28	VSS_95	1AB2
PWR_CTRL3/I2C6_SDA_M0/GPIO0_A5_d	Y29	LP4_DQS1N_A/LP4X_DQS1N_A/LP5_RDQS1N_A	1AB3
UART0_RX_M0/JTAG_TMS_M1/GPIO0_D5_u	AA28	LP4_DQS1P_A/LP4X_DQS1P_A/LP5_RDQS1P_A	1AB4
LP4_DQ7_A/LP4X_DQ7_A/LP5_DQ7_A	AB1	VSS_96	1AB5
I2C0_SCL_M1/UART8_TX_M2/I3C0_SCL_M0/GPIO0_C1_d	AB28	VSS_97	1AB6
I2C2_SDA_M0/UART1_RX_M0/CPULIT_AVS/PWM1_CH3_M0/GPIO0_C0_d	AB29	AVSS_10	1AB20
LP4_DQ6_A/LP4X_DQ6_A/LP5_DQ6_A	AC1	AVSS_11	1AB21
SAI0_SDI1_M1/SAI0_SDO3_M1/PDM0_SDI1_M0/SPI0_MISO_M0/GPIO0_D1_d	AC28	AVSS_12	1AB22
REF_CLK1_OUT/I2C1_SCL_M1/UART4_TX_M2/PWM1_CH0_M0/GPIO0_B4_d	AD28	AVSS_13	1AB23
REF_CLK2_OUT/I2C1_SDA_M1/UART4_RX_M2/PWM1_CH1_M0/GPIO0_B5_d	AD29	AVSS_14	1AB24
LP4_DMI1_A/LP4X_DMI1_A/LP5_DMI1_A	AE1	VSS_98	1AC1
MIPI_DPHY_CSI1_RX_D0N	AE28	VSS_99	1AC2
MIPI_DPHY_CSI1_RX_D0P	AE29	VSS_100	1AC3
LP4_DQ8_A/LP4X_DQ8_A/LP5_DQ8_A	AF1	VSS_101	1AC4
MIPI_DPHY_CSI1_RX_D1N	AF28	VSS_102	1AC5
MIPI_DPHY_CSI1_RX_D1P	AF29	UFS_TX_D0N	1AC6
MIPI_DPHY_CSI1_RX_D2N/MIPI_DPHY_CSI2_RX_D0N	AG28	AVSS_15	1AC20
MIPI_DPHY_CSI1_RX_D2P/MIPI_DPHY_CSI2_RX_D0P	AG29	AVSS_16	1AC21
LP4_DQ11_A/LP4X_DQ11_A/LP5_DQ11_A	AH1	MIPI_DPHY_CSI1_RX_CLKP	1AC22
MIPI_DPHY_CSI1_RX_D3N/MIPI_DPHY_CSI2_RX_D1N	AH28	MIPI_DPHY_CSI1_RX_CLKN	1AC23
MIPI_DPHY_CSI1_RX_D3P/MIPI_DPHY_CSI2_RX_D1P	AH29	AVSS_17	1AC24
SAI4_SCLK_M2/VP2_SYNC_OUT/I2C6_SDA_M3/SPI4_CLK_M0/PWM2_CH3_M1/GPIO4_C7_d	AJ1	LP4_DQ10_A/LP4X_DQ10_A/LP5_DQ10_A	1AD1
HDMI_TX_D2P/EDP_TX_D2P	AJ28	UFS_RSTN/GPIO4_D0_d	1AD2
AVSS_0	AJ29	VSS_103	1AD3
ISP_FLASH_TRIGOUT_M1/SAI4_SDO_M2/VP0_SYNC_OUT/I2C3_SDA_M3/SPI4_MOSI_M0/UART6_RX_M3/PWM2_CH5_M1/GPIO4_C5_d	AK1	UFS_TX_D1P	1AD4
DSM_AUD_LN_M1/HDMI_TX_HPDIN_M0/I2C7_SDA_M3/EDP_TX_HPDIN_M0/UART11_RX_M2/PWM0_CH1_M1/GPIO4_C1_d	AK2	UFS_TX_D1N	1AD5
DSM_AUD_LP_M1/SAI4_MCLK_M2/HDMI_TX_CEC_M0/I2C7_SCL_M3/SPI4_CSN1_M0/UART11_TX_M2/PWM1_CH5_M1/GPIO4_C0_d	AK3	UFS_TX_D0P	1AD6
UFS_REFCLK/GPIO4_D1_d	AK4	AVSS_18	1AD20
OSC_UFS_XIN	AK5	MIPI_DPHY_CSI2_RX_CLKP	1AD21

Pin Name	Pin	Pin Name	Pin
AVSS_1	AK6	MIPI_DPHY_CSI2_RX_CLKN	1AD22
UFS_RX_D1P	AK7	AVSS_19	1AD23
UFS_RX_D0P	AK8	AVSS_20	1AD24
USB2_OTG0_DP	AK9	SAI4_SDI_M2/VP1_SYNC_OUT/PCIE0_CLKREQN_M3/I2C6_SCL_M3/SPI4_MISO_M0/PWM2_CH2_M1/GPIO4_C6_d	1AE1
USB3_OTG0_SSRX1P/DP_TX_D0P	AK10	DSM_AUD_RN_M1/HDMI_TX_SDA/I2C2_SDA_M3/UART9_RX_M2/PWM2_CH1_M1/GPIO4_C3_d	1AE2
USB3_OTG0_SSTX1N/DP_TX_D1N	AK11	VSS_104	1AE3
USB3_OTG0_SSRX2P/DP_TX_D2P	AK12	AVSS_21	1AE4
USB3_OTG0_SSTX2N/DP_TX_D3N	AK13	AVSS_22	1AE6
AVSS_2	AK14	AVSS_23	1AE20
MIPI_DPHY_DSI_TX_D0N/MIPI_CPHY_DSI_TX_TRIO0_A	AK15	AVSS_24	1AE21
MIPI_DPHY_DSI_TX_D1N/MIPI_CPHY_DSI_TX_TRIO0_C	AK16	AVSS_25	1AE23
MIPI_DPHY_DSI_TX_CLKN/MIPI_CPHY_DSI_TX_TRIO1_B	AK17	HDMI_TX_D0P/EDP_TX_D0P	1AE24
MIPI_DPHY_DSI_TX_D2N/MIPI_CPHY_DSI_TX_TRIO2_A	AK18	VSS_105	2A1
MIPI_DPHY_DSI_TX_D3N/MIPI_CPHY_DSI_TX_TRIO2_C	AK19	VCCIO2_VCC	2A2
MIPI_DPHY_CSI0_RX_D0P/MIPI_CPHY_CSI_RX_TRIO0_B	AK20	VSS_106	2A3
MIPI_DPHY_CSI0_RX_D1P/MIPI_CPHY_CSI_RX_TRIO1_A	AK21	VCCIO5_VCC_0	2A4
MIPI_DPHY_CSI0_RX_CLKP/MIPI_CPHY_CSI_RX_TRIO1_C	AK22	VCCIO5_VCC_1	2A5
MIPI_DPHY_CSI0_RX_D2P/MIPI_CPHY_CSI_RX_TRIO2_B	AK23	VSS_107	2A6
MIPI_DPHY_CSI0_RX_D3P/NO_USE	AK24	VCCIO4_VCC	2A7
AVSS_3	AK25	VCCIO1_VCC	2A8
HDMI_TX_D3N/EDP_TX_D3N	AK26	VSS_108	2A9
HDMI_TX_D0N/EDP_TX_D0N	AK27	SARADC_AVDD1V8	2A10
HDMI_TX_D1P/EDP_TX_D1P	AK28	VSS_109	2A11
HDMI_TX_D2N/EDP_TX_D2N	AK29	VSS_110	2A12
VSS_6	AL1	VSS_111	2B1
DSM_AUD_RP_M1/HDMI_TX_SCL/I2C2_SCL_M3/UART9_TX_M2/PWM2_CH0_M1/GPIO4_C2_d	AL2	DDRPHY_CKE_VDDQ	2B2
ISP_PRELIGHT_TRIG_M1/SAI4_LRCK_M2/DP_HPDIN_M0/I2C3_SCL_M3/SPI4_CSN0_M0/UART6_TX_M3/PWM2_CH6_M1/GPIO4_C4_d	AL3	VSS_112	2B3
AVSS_4	AL4	VSS_113	2B4
OSC_UFS_XOUT	AL5	VSS_114	2B5
UFS_RX_D1N	AL6	VSS_115	2B6
UFS_RX_D0N	AL7	VSS_116	2B7
AVSS_5	AL8	VSS_117	2B8
USB2_OTG0_DM	AL9	VSS_118	2B9
USB3_OTG0_SSRX1N/DP_TX_D0N	AL10	VCCIO3_VCC	2B10
USB3_OTG0_SSTX1P/DP_TX_D1P	AL11	VSS_119	2B11
USB3_OTG0_SSRX2N/DP_TX_D2N	AL12	VSS_120	2B12
USB3_OTG0_SSTX2P/DP_TX_D3P	AL13	VSS_121	2C1
AVSS_6	AL14	DDRPHY_PLL_AVSS	2C2

Pin Name	Pin	Pin Name	Pin
MIPI_DPHY_DSI_TX_D0P/MIPI_CPHY_DSI_TX_TRIO0_B	AL15	DDRPHY_PLL_DVDD	2C3
MIPI_DPHY_DSI_TX_D1P/MIPI_CPHY_DSI_TX_TRIO1_A	AL16	GPU_DVDD_0	2C4
MIPI_DPHY_DSI_TX_CLKP/MIPI_CPHY_DSI_TX_TRIO1_C	AL17	GPU_DVDD_1	2C5
MIPI_DPHY_DSI_TX_D2P/MIPI_CPHY_DSI_TX_TRIO2_B	AL18	VSS_122	2C6
MIPI_DPHY_DSI_TX_D3P/NO_USE	AL19	NPU_DVDD_0	2C7
MIPI_DPHY_CSI0_RX_D0N/MIPI_CPHY_CSI_RX_TRIO0_A	AL20	NPU_DVDD_1	2C8
MIPI_DPHY_CSI0_RX_D1N/MIPI_CPHY_CSI_RX_TRIO0_C	AL21	NPU_DVDD_2	2C9
MIPI_DPHY_CSI0_RX_CLKN/MIPI_CPHY_CSI_RX_TRIO1_B	AL22	VSS_123	2C10
MIPI_DPHY_CSI0_RX_D2N/MIPI_CPHY_CSI_RX_TRIO2_A	AL23	VSS_124	2C11
MIPI_DPHY_CSI0_RX_D3N/MIPI_CPHY_CSI_RX_TRIO2_C	AL24	VSS_125	2C12
AVSS_7	AL25	DDRPHY_CK_VDDQ	2D1
HDMI_TX_D3P/EDP_TX_D3P	AL26	DDRPHY_PLL_AVDD1V8	2D2
HDMI_TX_D1N/EDP_TX_D1N	AL28	VSS_126	2D3
AVSS_8	AL29	GPU_DVDD_2	2D4
LP4_DQ8_B/LP4X_DQ8_B/LP5_DQ8_B	1A1	GPU_DVDD_3	2D5
VSS_7	1A2	VSS_127	2D6
VSS_8	1A3	NPU_DVDD_3	2D7
SPDIF_TX0_M0/FLEXBUS0_D15_M1/UART2_TX_M1/I2C3_SCL_M0/PCIE0_CLKREQN_M2/GPIO4_B5_d	1A4	NPU_DVDD_4	2D8
SAI1_SDO1_M0/SAI1_SDI3_M0/PDM1_CLK1_M1/FLEXBUS1_D13_M1/SPI4_CLK_M2/UART5_TX_M1/UART6_RTSN_M0/UART2_RTSN_M1/GPIO4_B0_d	1A5	VSS_128	2D9
SAI1_SDI0_M0/SAI4_SDO_M0/PDM1_SDI0_M1/SPI4_CSN0_M2/SPI3_CSN1_M2/PWM2_CH7_M0/GPIO4_B3_d	1A6	AVSS1_23	2D10
VO_LCDC_D21/PDM1_SDI2_M2/FLEXBUS0_D6/UART1_RX_M2/UART10_CTSN_M0/PWM1_CH2_M3/GPIO3_A6_d	1A7	MIPI_DPHY_CSI3/4_RX_AVDD0V75	2D11
VO_LCDC_D8/SAI2_LRCK_M2/FLEXBUS0_D10/FLEXBUS0_CSN_M2/UART11_CTSN_M0/SPI4_MOSI_M1/I2C9_SDA_M3/PWM2_CH1_M3/GPIO3_C3_d	1A8	MIPI_DPHY_CSI3/4_RX_AVDD1V8	2D12
VO_LCDC_D14/SPDIF_TX1_M0/FLEXBUS0_D0/UART9_CTSN_M1/PWM1_CH5_M3/GPIO3_B5_d	1A9	DDRPHY_VDDQ_0	2E1
VO_LCDC_D1/SAI2_SDI_M2/FLEXBUS0_D12/FLEXBUS1_D15_M0/FLEXBUS0_CSN_M3/UART2_RTSN_M2/SPI4_CSN1_M1/I3C1_SDA_M2/PWM2_CH4_M3/GPIO3_D2_d	1A10	DDRPHY_DVDD_0	2E2
VO_LCDC_D18/PDM1_CLK0_M2/FLEXBUS0_D4/UART10_TX_M0/SPI4_CSN0_M1/PWM1_CH3_M3/GPIO3_B1_d	1A11	VSS_129	2E3
VO_LCDC_D2/SAI2_MCLK_M2/FLEXBUS0_D11/FLEXBUS1_CSN_M2/SPI4_CLK_M1/I3C1_SDA_PU_M2/GPIO3_D1_d	1A12	GPU_DVDD_4	2E4
VI_CIF_D1/SAI2_SDO_M1/PDM1_SDI0_M0/UART11_TX_M1/SPI1_CSN0_M1/PWM1_CH3_M2/GPIO2_C4_d	1A13	VSS_130	2E5
SAI4_SCLK_M3/UART4_CTSN_M0/I2C5_SCL_M2/PWM1_CH5_M2/GPIO2_C6_d	1A14	VSS_131	2E6

Pin Name	Pin	Pin Name	Pin
VI_CIF_D4/SAI2_MCLK_M1/PDM1_CLK1_M0/UART9_TX_M0/SPI1_CSN1_M1/PWM1_CH1_M2/GPIO2_C1_d	1A15	LOGIC_DVDD_0	2E7
SAI4_SDO_M3/UART4_RX_M0/I2C6_SDA_M2/PWM2_CH1_M2/GPIO2_D1_d	1A16	VSS_132	2E8
VI_CIF_D11/SDMMC1_CMD_M1/SAI0_SDI2_M0/PDM0_SDI1_M3/UART1_CTSN_M1/SPI4_CSN0_M3/PCIE0_CLKREQN_M0/GPIO2_B2_d	1A17	VSS_133	2E9
VI_CIF_D12/SDMMC1_D3_M1/SAI0_SDI1_M0/PDM0_SDI2_M3/UART1_RX_M1/GPIO2_B1_d	1A18	AVSS1_24	2E10
VI_CIF_CLKI/SAI3_SDI_M2/SPDIF_TX1_M1/UART3_RTSN_M0/SPI3_CSN0_M0/GPIO3_A3_d	1A19	AVDD0V85	2E11
VI_CIF_CLKO/SAI3_SDO_M2/SPDIF_RX1_M1/UART3_CTSN_M0/SPI3_MISO_M0/MIPI_TE_M1/GPIO3_A2_d	1A20	AVDD1V8	2E12
SDMMC0_CMD/FSPI1_CSN0_M0/SAI3_SDO_M3/UART5_RX_M2/I2C5_SDA_M0/SPI0_CSN0_M1/PWM2_CH4_M0/GPIO2_A4_d	1A21	DDRPHY_VDDQ_1	2F1
SARADC_IN1	1A22	DDRPHY_VDDQ_2	2F2
SDMMC1_D2_M0/SAI3_SDO_M1/UART3_CTSN_M2/SPI1_MISO_M0/PCIE0_CLKREQN_M1/GPIO1_B6_d	1A23	DDRPHY_DVDD_1	2F3
SAI2_LRCK_M0/I3C0_SCL_M1/PWM1_CH3_M1/GPIO1_D2_d	1A24	VSS_134	2F4
LP4_DMI1_B/LP4X_DMI1_B/LP5_DMI1_B	1B1	VSS_135	2F5
VSS_9	1B2	VSS_136	2F6
LP4_DQ5_B/LP4X_DQ5_B/LP5_DQ5_B	1B3	LOGIC_MEM_DVDD_0	2F7
SAI4_LRCK_M0/PDM1_CLK0_M1/FLEXBUS0_D14_M1/SPI3_MISO_M2/UART6_RX_M0/I2C4_SDA_M1/GPIO4_A6_d	1B5	LOGIC_DVDD_1	2F8
SAI1_LRCK_M0/FLEXBUS1_D12_M1/SPI4_CSN1_M2/UART5_CTSN_M1/I2C2_SDA_M2/GPIO4_A5_d	1B6	LOGIC_DVDD_2	2F9
VO_POST_EMPTY/SPDIF_TX0_M1/CAM_CLK2_OUT_M0/SAI4_SDO_M1/FLEXBUS0_D14_M0/FLEXBUS1_D13_M0/FLEXBUS0_CSN_M1/UART3_RX_M1/I2C7_SDA_M2/GPIO4_A1_d	1B7	TSADC_TEST_OUT_TS	2F10
VO_LCDC_D6/SAI1_SDO0_M1/FLEXBUS1_D6/UART8_RX_M0/SPI1_MISO_M2/PWM2_CH2_M3/GPIO3_C5_d	1B9	PCIE0_AVDD0V85	2F11
VO_LCDC_D10/SAI1_SDO2_M1/FLEXBUS1_D8/UART11_RX_M0/SPI2_MISO_M2/I2C5_SDA_M3/GPIO3_C1_d	1B10	PCIE0_AVDD1V8	2F12
SPDIF_RX0_M1/CAM_CLK1_OUT_M0/SAI4_LRCK_M1/FLEXBUS0_D13_M0/FLEXBUS1_D14_M0/FLEXBUS1_CSN_M3/UART3_TX_M1/SPI1_CSN1_M2/I2C7_SCL_M2/MIPI_TE_M2/GPIO4_A0_d	1B12	DDRPHY_VDDQ_3	2G1
ISP_PRELIGHT_TRIG_M0/UART6_RTSN_M1/I2C9_SDA_M2/PWM2_CH4_M2/GPIO2_D4_d	1B13	DDRPHY_DVDD_2	2G2
ISP_FLASH_TRIGOUT_M0/UART6_CTSN_M1/I2C9_SCL_M2/PWM2_CH5_M2/GPIO2_D5_d	1B15	DDRPHY_DVDD_3	2G3
VI_CIF_D10/SDMMC1_CLK_M1/SAI0_SDO2_M0/PDM0_CLK1_M3/UART1_RTSN_M1/SPI4_CLK_M3/GPIO2_B3_d	1B16	VSS_137	2G4
VI_CIF_VSYNC/SAI3_LRCK_M2/UART3_RX_M0/SPI3_MOSI_M0/I2C7_SDA_M1/GPIO3_A1_d	1B18	CPU_BIG_DVDD_0	2G5
SARADC_IN2	1B19	CPU_BIG_DVDD_1	2G6
SDMMC0_CLK/FSPI1_CLK_M0/SAI3_SCLK_M3/TEST_CLK_OUT/UART5_TX_M2/I2C5_SCL_	1B21	VSS_138	2G7

Pin Name	Pin	Pin Name	Pin
M0/SPI0_CLK_M1/I3C1_SDA_PU_M1/GPIO2_A5_d			
SDMMC1_CLK_M0/SAI3_MCLK_M1/PDM0_CLK0_M2/UART3_RX_M2/GPIO1_C1_d	1B22	LOGIC_DVDD_3	2G8
FSPI1_D0_M1/UART4_TX_M1/UART2_RTSN_M0/SPI2_MOSI_M1/GPIO1_C4_d	1B23	LOGIC_DVDD_4	2G9
EMMC_D7/SAI0_SDO0_M2/SAI3_SDI_M0/SPI0_CLK_M2/GPIO1_A7_u	1B24	VSS_139	2G10
LP4_DQ13_B/LP4X_DQ13_B/LP5_DQ13_B	1C1	PLL_DVDD0V75	2G11
VSS_10	1C2	PLL_AVSS	2G12
LP4_DQ4_B/LP4X_DQ4_B/LP5_DQ4_B	1C3	DDRPHY_VDDQ_4	2H1
VSS_11	1C4	DDRPHY_DVDD_4	2H2
SAI4_SCLK_M0/PDM1_SDI3_M1/FLEXBUS0_D13_M1/SPI3_MOSI_M2/UART6_TX_M0/I2C4_SCL_M1/GPIO4_A4_d	1C5	VSS_140	2H3
SAI1_SCLK_M0/FLEXBUS1_CSN_M4/SPI3_CSN0_M2/UART5_RTSN_M1/I2C2_SCL_M2/PWM2_CH4_M1/GPIO4_A3_d	1C6	CPU_LIT_DVDD_0	2H4
VO_LCDC_D4/SAI1_SCLK_M1/FLEXBUS1_D4/UART8_RTSN_M0/SPI1_CLK_M2/GPIO3_C7_d	1C7	VSS_141	2H5
VSS_12	1C9	CPU_BIG_DVDD_2	2H6
VO_LCDC_VSYNC/SAI1_SDI3_M1/FLEXBUS1_CLK/UART5_CTSN_M0/SPI3_MOSI_M1/PWM2_CH6_M3/GPIO3_D6_d	1C10	CPU_BIG_DVDD_3	2H7
VO_LCDC_D3/SAI1_MCLK_M1/FLEXBUS1_D3/UART8_CTSN_M0/SPI1_CSN0_M2/PWM2_CH3_M3/GPIO3_D0_d	1C12	LOGIC_DVDD_5	2H8
VSS_13	1C13	LOGIC_DVDD_6	2H9
VI_CIF_D0/SAI2_SDI_M1/PDM1_CLK0_M0/UART11_RX_M1/SPI1_CLK_M1/PWM1_CH4_M2/GPIO2_C5_d	1C15	TVSS	2H10
VSS_14	1C16	OTP_DVDD0V75	2H11
VI_CIF_D8/SDMMC1_DETN_M1/SAI0_MCLK_M0/PDM0_CLK0_M3/UART7_RTSN_M0/SPI4_MISO_M3/GPIO2_B5_d	1C18	PLL_AVDD1V8	2H12
SARADC_IN3	1C19	VSS_142	2J1
VSS_15	1C21	DDRPHY_VDDQ_5	2J2
FSPI1_D3_M1/PDM0_SDI1_M2/UART2_RX_M0/I2C8_SDA_M1/GPIO1_C7_d	1C22	CPU_LIT_DVDD_1	2J3
SDMMC1_DETN_M0/FSPI1_CSN0_M1/UART4_CTSN_M1/I2C6_SDA_M1/SPI2_CSN0_M1/GPIO1_C3_u	1C23	CPU_LIT_DVDD_2	2J4
EMMC_D2/FSPI0_D2/SAI0_SDO1_M2/SAI0_SDI3_M2/PDM0_SDI3_M1/UART7_TX_M1/UART6_RTSN_M2/GPIO1_A2_u	1C24	VSS_143	2J5
VSS_16	1D1	CPU_BIG_DVDD_4	2J6
LP4_DQ0_B/LP4X_DQ0_B/LP5_DQ0_B	1D2	CPU_BIG_DVDD_5	2J7
VSS_17	1D3	VSS_144	2J8
LP5_WCK1P_B	1D4	LOGIC_MEM_DVDD_1	2J9
VSS_18	1D5	OSC_AVDD1V8	2J10
SAI1_MCLK_M0/SAI4_MCLK_M0/AUPLL_CLK_IN_M2/PWM2_CH5_M0/GPIO4_A2_d	1D6	VSS_145	2J11
VO_LCDC_D5/SAI1_LRCK_M1/FLEXBUS1_D5/UART8_TX_M0/SPI1_MOSI_M2/GPIO3_C6_d	1D7	VSS_146	2J12
VO_LCDC_D7/SAI1_SDO1_M1/FLEXBUS1_D7/UART11_TX_M0/SPI2_CSN0_M2/I2C5_SCL_M3/GPIO3_C4_d	1D9	VSS_147	2K1
VO_LCDC_HSYNC/SAI1_SDI2_M1/FLEXBUS1_D0/UART5_TX_M0/SPI3_MISO_M1/I2C3_SDA_M2/GPIO3_D5_d	1D10	VSS_148	2K2

Pin Name	Pin	Pin Name	Pin
VO_LCDC_D12/SAI1_SDI0_M1/FLEXBUS1_D10/FLEXBUS1_CSN_M0/UART2_RX_M2/UART3_CTSN_M1/I2C4_SDA_M3/GPIO3_B7_d	1D12	CPU_LIT_DVDD_3	2K3
VO_LCDC_D23/SAI4_SDI_M1/FLEXBUS1_D11/FLEXBUS0_CSN_M0/UART1_CTSN_M2/SPI2_CLK_M2/PWM1_CH0_M3/GPIO3_A4_d	1D13	CPU_LIT_DVDD_4	2K4
VI_CIF_D3/SAI2_SCLK_M1/PDM1_SDI2_M0/UART11_CTSN_M1/SPI1_MOSI_M1/PWM1_CH2_M2/GPIO2_C2_d	1D15	VSS_149	2K5
VI_CIF_HREF/SAI3_SCLK_M2/UART3_TX_M0/SPI3_CLK_M0/I2C7_SCL_M1/GPIO3_A0_d	1D16	CPU_BIG_DVDD_6	2K6
CAM_CLK1_OUT_M1/SAI3_MCLK_M2/SPDIF_RX0_M2/UART9_RTSN_M0/I3C1_SDA_PU_M0/PWM2_CH6_M2/GPIO2_D6_d	1D18	CPU_BIG_DVDD_7	2K7
SARADC_IN5	1D19	VSS_150	2K8
SARADC_IN6	1D21	VSS_151	2K9
SAI2_SCLK_M0/UART10_RX_M1/I3C0_SDA_PU_M1/GPIO1_D1_d	1D22	VSS_152	2K10
EMMC_RSTN/FSPI0_CSN0/UART6_RX_M2/I2C7_SDA_M0/MIPI_TE_M3/PWM2_CH1_M0/GPIO1_B3_u	1D23	PMUIO0_VCC1V8	2K11
EMMC_D4/SAI0_MCLK_M2/SAI3_MCLK_M0/SPI0_CSN0_M2/GPIO1_A4_u	1D24	VSS_153	2K12
LP4_DQ12_B/LP4X_DQ12_B/LP5_DQ12_B	1E1	VSS_154	2L1
VSS_19	1E2	PMU_LOGIC_DVDD0V75_0	2L2
VSS_20	1E3	VSS_155	2L3
LP5_WCK1N_B	1E4	VSS_156	2L4
VSS_21	1E5	VSS_157	2L5
VSS_22	1E6	VSS_158	2L6
VO_LCDC_CLK/CAM_CLK0_OUT_M0/SAI4_SCLK_M1/FLEXBUS0_D15_M0/FLEXBUS1_D12_M0/FLEXBUS1_CSN_M1/UART5_RTSN_M0/SPI3_CSN1_M1/PWM2_CH7_M3/GPIO3_D7_d	1E7	VSS_159	2L7
VO_LCDC_D11/SAI1_SDO3_M1/FLEXBUS1_D9/UART2_TX_M2/UART3_RTSN_M1/I2C4_SCL_M3/GPIO3_C0_d	1E9	VSS_160	2L8
VSS_23	1E10	VSS_161	2L9
VO_LCDC_DEN/SAI1_SDI1_M1/FLEXBUS1_D1/UART5_RX_M0/SPI3_CLK_M1/I2C3_SCL_M2/GPIO3_D4_d	1E12	PMU_LOGIC_DVDD0V75_1	2L10
VSS_24	1E13	MIPI_DPHY_CSI1/2_RX_AVDD0V75	2L11
CAM_CLK2_OUT_M1/SAI0_SDO3_M0/SPDIF_TX0_M2/UART9_CTSN_M0/SPI3_CSN1_M0/PWM2_CH7_M2/GPIO2_D7_d	1E15	VSS_162	2L12
VSS_25	1E16	AVSS_26	2M1
SARADC_IN4	1E18	OSC_UFS_AVDD	2M2
SARADC_IN7	1E19	VCCIO7_VCC	2M3
SAI2_MCLK_M0/PDM0_SDI3_M2/SPDIF_RX1_M2/UART10_RTSN_M1/I2C5_SCL_M1/GPIO1_D4_d	1E21	AVSS_27	2M4
FSPI1_CLK_M1/PDM0_CLK1_M2/SPDIF_TX1_M2/UART10_CTSN_M1/I2C5_SDA_M1/SPI2_CLK_M1/CLK1_32K_OUT/GPIO1_D5_d	1E22	USB3_OTG0_DP_TX_AVDD0V85	2M5
VSS_26	1E23	AVSS_28	2M6
VSS_27	1E24	MIPI_DCPHY_AVDD	2M7
LP4_DQS0N_B/LP4X_DQS0N_B/LP5_RDQS0N_B	1F1	MIPI_DCPHY_AVDD1V2	2M8
LP4_DQ1_B/LP4X_DQ1_B/LP5_DQ1_B	1F2	AVSS_29	2M9
VSS_28	1F3	AVSS_30	2M10

Pin Name	Pin	Pin Name	Pin
LP4_A4_B/LP4X_A4_B/LP5_A4_B	1F4	AVSS_31	2M11
VSS_29	1F5	AVSS_32	2M12
VSS_30	1F6	AVSS_33	2N1
VSS_31	1F20	UFS_AVDD0V85	2N2
VSS_32	1F21	VCCIO6_VCC	2N3
EMMC_CMD/FSPI0_RSTN/FSPI0_CSN1/UART6_TX_M2/I2C7_SCL_M0/GPIO1_B0_u	1F22	USB3_OTG0_DP_TX_AVDD1V8	2N4
EMMC_STRB/SAI0_SDI0_M2/SAI3_SDO_M0/PDM0_SDI0_M1/SPI0_CSN1_M2/GPIO1_B2_d	1F23	USB3_OTG0_DP_TX_DVDD0V85	2N5
VSS_33	1F24	AVSS_34	2N6
LP4_DQ2_B/LP4X_DQ2_B/LP5_DQ2_B	1G1	MIPI_DCPHY_VREG	2N7
LP4_A3_B/LP4X_A3_B/LP5_A3_B	1G2	AVSS_35	2N8
VSS_34	1G3	AVSS_36	2N9
LP5_WCK0N_B	1G4	HDMI_TX_EDP_TX_AVDDIO1V8	2N10
LP5_WCK0P_B	1G5	HDMI_TX_EDP_TX_AVDDD0V75	2N11
VSS_35	1G6	AVSS_37	2N12
VSS_36	1G20	AVSS_38	2P1
VSS_37	1G21	UFS_AVDD1V8	2P2
VSS_38	1G22	USB2_OTG0_VBUSDET	2P3
EMMC_CLK/FSPI0_CLK/SAI0_SDO3_M2/SAI0_SDI1_M2/PDM0_CLK0_M1/PWM2_CH7_M1/GPIO1_B1_d	1G23	USB2_OTG_AVDD1V8	2P4
VSS_39	1G24	USB2_OTG_DVDD0V75	2P5
VSS_40	1H1	AVSS_39	2P6
VSS_41	1H2	USB2_OTG_AVDD3V3	2P7
VSS_42	1H3	MIPI_DCPHY_AVDD1V8	2P8
VSS_43	1H4	AVSS_40	2P9
LP5_A6_B	1H5	HDMI_TX_EDP_TX_AVDDCMN1V8	2P10
VSS_44	1H6	HDMI_TX_EDP_TX_AVDDC0V75	2P11
VSS_45	1H20	AVSS_41	2P12
AVSS1_3	1H21	AVSS_42	2R1
MIPI_DPHY_CSI3_RX_CLKP	1H22	UFS_TX_REXT	2R2
MIPI_DPHY_CSI3_RX_CLKN	1H23	USB2_OTG0_REXT	2R3
AVSS1_4	1H24	AVSS_43	2R4
LP4_A1_B/LP4X_A1_B/LP5_A1_B	1J1	AVSS_44	2R5
VSS_46	1J2	USB2_OTG0_ID	2R6
LP4_A2_B/LP4X_A2_B/LP5_A2_B	1J3	AVSS_45	2R7
VSS_47	1J4	AVSS_46	2R8
LP4_CSN0_B/LP4X_CSN0_B	1J5	AVSS_47	2R9
ZQ_B	1J6	AVSS_48	2R10
VCCIO0_VCC1V8	1J20	AVSS_49	2R11
AVSS1_5	1J21	AVSS_50	2R12
AVSS1_6	1J22	AVSS_51	2T1
AVSS1_7	1J23	DP_TX_AUXP	2T2
AVSS1_8	1J24	DP_TX_AUXN	2T3
LP4_CLKP_B/LP4X_CLKP_B/LP5_CLKP_B	1K1	USB2_OTG1_DP	2T4
LP4_CKE0_B/LP4X_CKE0_B/LP5_CSN0_B	1K2	USB2_OTG1_DM	2T5
VSS_48	1K3	AVSS_52	2T6
LP4_CSN1_B/LP4X_CSN1_B	1K4	USB3_OTG0_REXT/DP_TX_REXT	2T7
LP4_A5_B/LP4X_A5_B/LP5_A5_B	1K5	AVSS_53	2T8

Pin Name	Pin	Pin Name	Pin
VSS_49	1K6	USB2_OTG1_ID	2T9
AVSS1_9	1K20	USB2_OTG1_VBUSDET	2T10
AVSS1_10	1K21	AVSS_54	2T11
MIPI_DPHY_CSI4_RX_CLKP	1K22	HDMI_TX_SBDP/EDP_TX_AUXP	2T12
MIPI_DPHY_CSI4_RX_CLKN	1K23	AVSS_55	2U1
AVSS1_11	1K24	AVSS_56	2U2
LP4_CLKP_A/LP4X_CLKP_A/LP5_CLKP_A	1L1	AVSS_57	2U3
VSS_50	1L2	AVSS_58	2U4
VSS_51	1L3	AVSS_59	2U5
VSS_52	1L4	AVSS_60	2U6
VSS_53	1L5	AVSS_61	2U7
VSS_54	1L6	USB2_OTG1_REXT	2U8
AVSS1_12	1L20	AVSS_62	2U9
AVSS1_13	1L21	AVSS_63	2U10
AVSS1_14	1L22	AVSS_64	2U11
N/A	1L23	HDMI_TX_SBDN/EDP_TX_AUXN	2U12
AVSS1_15	1L24	AVSS_65	2V1
VSS_55	1M1	AVSS_66	2V2
VSS_56	1M2	AVSS_67	2V3
LP4_CKE1_B/LP4X_CKE1_B/LP5_CSN1_B	1M3	AVSS_68	2V4
VSS_57	1M4	AVSS_69	2V5
LP4_A4_A/LP4X_A4_A/LP5_A4_A	1M5	AVSS_70	2V6
VSS_58	1M6	AVSS_71	2V7
AVSS1_16	1M20	AVSS_72	2V8
AVSS1_17	1M21	AVSS_73	2V9
AVSS1_18	1M22	AVSS_74	2V10
N/A	1M23	AVSS_75	2V11
AVSS1_19	1M24	AVSS_76	2V12

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The table below provides the absolute ratings.

Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute Ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU	CPU_BIG_DVDD CPU_LIT_DVDD	-0.3	1.1	V
Supply voltage for GPU	GPU_DVDD	-0.3	1.1	V
Supply voltage for NPU	NPU_DVDD	-0.3	1.1	V
Supply voltage for core logic	LOGIC_DVDD	-0.3	0.95	V
Supply voltage for core memory	LOGIC_MEM_DVDD	-0.3	0.95	V
0.75V supply voltage	PMU_LOGIC_DVDD0V75 PLL_DVDD0V75 USB2_OTG_DVDD0V75 HDMI_TX_EDP_TX_AVDDD0V75 HDMI_TX_EDP_TX_AVDDC0V75 MIPI_DPHY_CSI1/2_RX_AVDD0V75 MIPI_DPHY_CSI3/4_RX_AVDD0V75 OTP_DVDD0V75	-0.3	0.95	V
0.85V supply voltage	DDRPHY_DVDD DDRPHY_PLL_DVDD USB3_OTG0_DP_TX_DVDD0V85 USB3_OTG0_DP_TX_AVDD0V85 MIPI_DCPHY_VDD PCIE21_PORT0_AVDD0V85 AVDD0V85 UFS_AVDD0V85	-0.3	1.00	V
1.2V supply voltage	MIPI_DCPHY_AVDD_1V2	-0.3	1.35	V
1.8V supply voltage	OSC_AVDD1V8 DDRPHY_PLL_AVDD1V8 MIPI_DPHY_CSI1/2_RX_AVDD1V8 MIPI_DPHY_CSI3/4_RX_AVDD1V8 MIPI_DCPHY_AVDD1V8 HDMI_TX_EDP_TX_AVDDCMN1V8 HDMI_TX_EDP_TX_AVDDIO1V8 USB3_OTG0_DP_TX_AVDD1V8 USB2_OTG_AVDD1V8 PCIE21_PORT0_AVDD1V8 SARADC_AVDD1V8 PLL_AVDD1V8 UFS_AVDD1V8	-0.5	1.98	V
3.3V supply voltage	USB2_OTG_AVDD3V3	-0.5	3.63	V
1.8V only GPIO supply voltage	PMUIO0_VCC1V8 VCCIO0_VCC1V8	-0.5	1.98	V

1.8V/3.3V GPIO supply voltage	PMUIO1_VCC VCCIO1_VCC VCCIO2_VCC VCCIO3_VCC VCCIO4_VCC VCCIO5_VCC VCCIO6_VCC	-0.5	3.63	V
1.2V/1.8V supply voltage	OSC_UFS_AVDD VCCIO7_VCC	-0.5	1.98	V
Supply voltage for DDR IO (LPDDR4/4X 0.6V; LPDDR5 0.5V)	DDRPHY_VDDQ DDRPHY_CK_VDDQ	-0.3	0.7	V
Supply voltage for DDR IO (LPDDR4/4X 1.1V; LPDDR5 1.05V)	DDRPHY_CKE_VDDQ	-0.3	1.25	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj	NA	125	℃

3.2 Recommended Operating Conditions

The following table describes the recommended operating conditions.

Table 3-2 Recommended operating conditions

Parameters	Symbol	Min(1)	Typ	Max(1)	Unit
Voltage for CPU BigCore	CPU_BIG_DVDD	0.675	0.75	1.0	V
Voltage for CPU LitCore and CCI	CPU_LIT_DVDD	0.675	0.75	1.0	V
Voltage for GPU	GPU_DVDD	0.675	0.75	0.893	V
Voltage for NPU	NPU_DVDD	0.675	0.75	0.893	V
Voltage for Logic (Normal drive)	LOGIC_DVDD	0.675	0.75	0.825	V
Voltage for Logic (Under drive)(2)	LOGIC_DVDD	0.585	0.65	0.715	V
Voltage for Logic Memory	LOGIC_MEM_DVDD	0.675	0.75	0.825	V
Voltage for PMU	PMU_LOGIC_DVDD0V75	0.675	0.75	0.825	V
Digital GPIO Power (1.8V only)	PMUIO0_VCC1V8 VCCIO0_VCC1V8	1.65	1.8	1.95	V
Digital GPIO Power (3.3V/1.8V)	PMUIO1_VCC VCCIO1_VCC VCCIO2_VCC VCCIO3_VCC VCCIO4_VCC VCCIO5_VCC VCCIO6_VCC	2.7 1.65	3.3 1.8	3.6 1.95	V
Digital GPIO Power (1.8V/1.2V)	OSC_UFS_AVDD VCCIO7_VCC	1.08 1.65	1.2 1.8	1.32 1.95	V
DDR CH0 Logic power(0.75V)	DDRPHY_DVDD	0.675	0.75	0.9	V
DDR CH0_PLL power(0.75V)	DDRPHY_PLL_DVDD	0.675	0.75	0.8925	V
DDR CH0_PLL power(1.8V)	DDRPHY_PLL_AVDD1V8	1.62	1.8	1.98	V
LPDDR4 IO VDDQ power	DDRPHY_VDDQ DDRPHY_CK_VDDQ	0.57	0.6	0.65	V
LPDDR4 Retention IO VDDQ Power	DDRPHY_CKE_VDDQ	1.06	1.1	1.17	V
LPDDR5 IO VDDQ power	DDRPHY_VDDQ DDRPHY_CK_VDDQ	0.47	0.5	0.57	V
LPDDR5 Retention IO VDDQ Power	DDRPHY_CKE_VDDQ	1.01	1.05	1.12	V
PLL Analog Power(0.75V)	PLL_DVDD0V75	0.675	0.75	0.8925	V
PLL Analog Power(1.8V)	PLL_AVDD1V8	1.62	1.8	1.98	V
USB 2.0 Analog Power (0.75V)	USB2_OTG_DVDD0V75	0.6975	0.75	0.825	V

USB 2.0 Analog Power (1.8V)	USB2_OTG_AVDD1V8	1.674	1.8	1.98	V
USB 2.0 Analog Power (3.3V)	USB2_OTG_AVDD3V3	3.069	3.3	3.63	V
USB & DP Analog Power (0.85V)	USB3_OTG0_DP_TX_DVDD0V85	0.8075	0.85	0.8925	V
USB & DP Analog Power (1.8V)	USB3_OTG0_DP_TX_AVDD1V8	1.71	1.8	1.89	V
Combo PIPE PHY Analog Power(0.85V)	PCIE21_PORT0_AVDD0V85	0.8	0.85	0.935	V
Combo PIPE PHY Analog Power(1.8V)	PCIE21_PORT0_AVDD1V8	1.62	1.8	1.98	V
MIPI CSI DPHY Analog Power(0.75V)	MIPI_DPHY_CSI1/2_RX_AVDD0V75 MIPI_DPHY_CSI3/4_RX_AVDD0V75	0.675	0.75	0.825	V
MIPI CSI DPHY Analog Power(1.8V)	MIPI_DPHY_CSI1/2_RX_AVDD1V8 MIPI_DPHY_CSI3/4_RX_AVDD1V8	1.62	1.8	1.98	V
MIPI DCPHY Analog Power (0.85V)	MIPI_DCPHY_AVDD	0.8075	0.85	0.8925	V
MIPI DCPHY Analog Power (0.75V)	MIPI_DCPHY_AVDD	0.7125	0.75	0.7875	V
MIPI DCPHY Analog Power (1.2V)	MIPI_DCPHY_AVDD1V2	1.14	1.2	1.26	V
MIPI DCPHY Analog Power (1.8V)	MIPI_DCPHY_AVDD1V8	1.71	1.8	1.89	V
HDMI/eDP TX Digital Power (0.75V)	HDMI_TX_EDP_TX_AVDDD0V75	0.7125	0.75	0.85	V
HDMI/eDP TX Analog Power (0.75V)	HDMI_TX_EDP_TX_AVDDC0V75	0.7125	0.75	0.85	V
HDMI/eDP TX Analog Power (1.8V)	HDMI_TX_EDP_TX_AVDDCMN1V8	1.71	1.8	1.89	V
HDMI/eDP TX Analog Power (1.8V)	HDMI_TX_EDP_TX_AVDDIO1V8	1.71	1.8	1.89	V
UFS MPHY Analog Power (0.85V)	UFS_AVDD0V85	0.8075	0.85	0.8925	V
UFS MPHY Analog Power (1.8V)	UFS_AVDD1V8	1.71	1.8	1.89	V
SARADC Analog Power(1.8V)	SARADC_AVDD1V8	1.62	1.8	1.98	V
OTP Analog Power(0.75V)	OTP_DVDD0V75	0.675	0.75	0.825	V
OSC Analog Power(1.8V)	OSC_AVDD1V8	1.65	1.8	1.95	V
OSC input clock frequency		NA	24	NA	MHz
Max A72 CPU frequency		NA	NA	2.1	GHz
Max A53 CPU frequency		NA	NA	1.9	GHz
Max GPU frequency		NA	NA	800	MHz
Max NPU frequency		NA	NA	500	MHz
Ambient Operating Temperature	TA	0	NA	80	℃

Note (1):For all power supply inputs, the min and max voltage requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, and so forth.
Note (2):When LOGIC_DVDD works at under drive voltage, the frequency of modules in VD_LOGIC should lower down.

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital 3.3V/1.8V GPIO @3.3V	Input Low Voltage for CMOS operation	V_{IL}	VSS-0.3	NA	0.8	V
	Input High Voltage for CMOS operation	V_{IH}	2.0	NA	DVDD+0.3	V
	Input Low Voltage for Schmitt Trigger operation	V_{IL}	VSS-0.3	NA	0.7	V
	Input High Voltage for Schmitt Trigger operation	V_{IH}	2.1	NA	DVDD+0.3	V
	Output Low Voltage	V_{OL}	VSS	NA	0.25*DVDD	V

Parameters		Symbol	Min	Typ	Max	Unit
	Output High Voltage	V_{OH}	0.75*DVDD	NA	DVDD	V
	Pullup Resistor	R_{RPU}	10	NA	100	Kohm
	Pulldown Resistor	R_{RPD}	10	NA	100	Kohm
Digital 3.3V/1.8V GPIO @1.8V	Input Low Voltage	V_{IL}	VSS-0.3	NA	0.3*DVDD	V
	Input High Voltage	V_{IH}	0.7*DVDD	NA	DVDD+0.3	V
	Output Low Voltage	V_{OL}	VSS	NA	0.25*DVDD	V
	Output High Voltage	V_{OH}	0.75*DVDD	NA	DVDD	V
	Pullup Resistor	R_{RPU}	10	NA	50	Kohm
	Pulldown Resistor	R_{RPD}	10	NA	50	Kohm
Digital 1.8V only and Digital 1.8V/1.2V GPIO @1.8V	Input Low Voltage	V_{IL}	VSS-0.3	NA	0.3*DVDD	V
	Input High Voltage	V_{IH}	0.7*DVDD	NA	DVDD+0.3	V
	Output Low Voltage	V_{OL}	VSS	NA	0.25*DVDD	V
	Output High Voltage	V_{OH}	0.75*DVDD	NA	DVDD	V
	Pullup Resistor	R_{RPU}	10	NA	50	Kohm
	Pulldown Resistor	R_{RPD}	10	NA	50	Kohm
Digital 1.8V/1.2V GPIO @1.2V	Input Low Voltage	V_{IL}	VSS-0.3	NA	0.3*DVDD	V
	Input High Voltage	V_{IH}	0.7*DVDD	NA	DVDD+0.3	V
	Output Low Voltage	V_{OL}	VSS-0.3	NA	0.25*DVDD	V
	Output High Voltage	V_{OH}	0.75*DVDD	NA	DVDD+0.3	V
	Pullup Resistor	R_{RPU}	10	NA	100	Kohm
	Pulldown Resistor	R_{RPD}	10	NA	100	Kohm
VCCIO0 @1.8V	Input Low Voltage	V_{IL}	VSS	NA	0.35*DVDD	V
	Input High Voltage	V_{IH}	0.65*DVDD	NA	DVDD	V
	Output Low Voltage	V_{OL}	VSS	NA	0.45	V
	Output High Voltage	V_{OH}	DVDD-0.45	NA	DVDD	V
	Pullup Resistor	R_{RPU}	10	NA	50	Kohm
	Pulldown Resistor	R_{RPD}	10	NA	50	Kohm
DDR IO	Input Low Voltage	V_{IL}	NA	NA	Vref-0.14	V
	Input High Voltage	V_{IH}	Vref+0.14	NA	NA	V
	Output Log Voltage	V_{OL}	NA	NA	0.2	V
	Output High Voltage	V_{OH}	0.25	NA	NA	V
	Input Low Current	I_{IL}	-100/-500	NA	100/500	Room/Hot uA
	Input High Current	I_{IH}	-100/-500	NA	100/500	Room/Hot uA

Note: VDDO and DVDD are both IO power Supply

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital 3.3V/1.8V GPIO @3.3V	Input leakage current	I_{PAD}	DVDD=Max, V_{PAD}=0V or DVDD	-10	NA	10	uA
	Input Hysteresis for Schmitt Trigger Operation	V_H		0.2	NA	NA	V
	Input pullup resistor current	I_{RPU}	V_{PAD} = 0V	-20	NA	-180	uA

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
	Input pulldown resistor current	I_{RPD}	V_{PAD} = DVDD	20	NA	180	uA
Digital 3.3V/1.8V GPIO @1.8V	Input leakage current	I_{PAD}	DVDD=Max, V_{PAD}=0V or DVDD	-10	NA	10	uA
	Input Hysteresis for Schmitt Trigger Operation	V_H		0.1* DVDD	NA	NA	V
	Input pullup resistor current	I_{RPU}	V_{PAD} = 0V	-20	NA	-180	uA
	Input pulldown resistor current	I_{RPD}	V_{PAD} = DVDD	20	NA	180	uA
Digital 1.8V only and Digital 1.8V/1.2V GPIO @1.8V	Input leakage current	I_{PAD}	DVDD=Max, V_{PAD}=0V or DVDD	-10	NA	10	uA
	Input Hysteresis for Schmitt Trigger Operation	V_H		0.1* DVDD	NA	NA	V
	Input pullup resistor current	I_{RPU}	V_{PAD} = 0V	-20	NA	-170	uA
	Input pulldown resistor current	I_{RPD}	V_{PAD} = DVDD	20	NA	170	uA
Digital 1.8V/1.2V GPIO @1.2V	Input leakage current	I_{PAD}	DVDD=Max, V_{PAD}=0V or DVDD	-10	NA	10	uA
	Input Hysteresis for Schmitt Trigger Operation	V_H		0.1* DVDD	NA	NA	V
	Input pullup resistor current	I_{RPU}	V_{PAD} = 0V	-10	NA	-100	uA
	Input pulldown resistor current	I_{RPD}	V_{PAD} = DVDD	10	NA	100	uA
VCCIO0 IO @1.8V	Input leakage current	I_{PAD}	DVDD=Max, V_{PAD}=0V or DVDD	-10	NA	10	uA
	Input Hysteresis for Schmitt Trigger Operation	V_H		0.1* DVDD	NA	NA	V
	Input pullup resistor current	I_{RPU}	V_{PAD} = 0V	-20	NA	-170	uA
	Input pulldown resistor current	I_{RPD}	V_{PAD} = DVDD	20	NA	170	uA

Note: VDDO and DVDD are both IO power Supply

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for INT PLL

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input clock frequency	F_{FIN}		4.5	-	300	MHz
Reference frequency(F_{FIN}/p)	F_{FREE}		4.5	7	12	MHz
Frequency of PLL's output	F_{FOUT}		35.2	-	4500	MHz
Frequency of VCO's output	F_{FVCO}		2250	-	4500	MHz
Lock time	T_{LT}	Measured at all F_{FIN} and F_{FOUT} range. RESETB=High	-	-	150	Cycles

Table 3-6 Electrical Characteristics for FRAC PLL

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input clock frequency	F_{FIN}		4.5	-	300	MHz

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Reference frequency(F_{FIN}/p)	F_{FREE}		4.5	20	30	MHz
Frequency of PLL's output	F_{FOUT}		35.2	-	4500	MHz
Frequency of VCO's output	F_{FVCO}		2250	-	4500	MHz
Lock time	T_{LT}	Measured at all F_{FIN} and F_{FOUT} range. RESETB=High	-	-	500	Cycles

Table 3-7 Electrical Characteristics for DDR PLL

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input clock frequency	F_{FIN}		6	-	300	MHz
Reference frequency(F_{FIN}/p)	F_{FREE}		6	20	30	MHz
Frequency of PLL's output	F_{FOUT}		51.6	-	6600	MHz
Frequency of VCO's output	F_{FVCO}		3300	-	6600	MHz
Lock time	T_{LT}	Measured at all F_{FIN} and F_{FOUT} range. RESETB=High	-	-	500	Cycles

Notes:

① *p is the input divider value*

3.6 Electrical Characteristics for PCIe2 Interface

Table 3-8 Electrical Characteristics for PCIe2 Interface

Parameters	Symbol	Min	Typ	Max	Unit
Transmitter					
Differential Peak-Peak TX Output Voltage Swing	$V_{TX\_DIFF\_PP}$	800	1000	1200	mV
Differential Peak-Peak Low Power TX Output Voltage Swing	$V_{TX\_DIFF\_PP\_LOW}$	400	NA	1200	mV
The output impedance	$R_{TX\_DIFF\_DC}$	80	100	120	ohm
Single Ended Output Resistance Matching	$R_{TX\_DC\_OFFSET}$	NA	NA	5	%
Transmitter output common mode voltage	$V_{TX\_DC\_CM}$	400	NA	800	mV
Maximum mismatch between TXP and TXM for both time and amp	$V_{TX\_CM\_AC\_PP\_ACTIVE}$	NA	NA	50	mV
The amount of voltage change allowed during Receiver Detection	$V_{TX\_RCV\_DETECT}$	NA	NA	600	mV
TX de-emphasis	$V_{TX\_DE\_RATIO}$	3.0	3.5	4.0	dB
AC Coupling Capacitor(USB3.2 Gen1x1/PCIe)	$C_{AC\_COUPLING}$	75	NA	200	nF
Output rising time for 20% to 80%	T_r	25	NA	NA	ps
Output falling time for 20% to 80%	T_f	25	NA	NA	ps
Transmitter short circuit limit	I_{TX_SHORT}	NA	NA	20	mA
Output differential skew	T_{SKEW_DIFF}	-15	NA	15	ps
Receiver					
Input Voltage Swing	V_{RXDPP_C}	250	NA	1200	mVpp
The input differential impedance	R_{RXD_C}	80	100	120	Ohm
Single Ended input Resistance Matching	$R_{RXD\_C\_MS}$	NA	NA	5	%

3.7 Electrical Characteristics for MIPI CDPHY interface

Table 3-9 Electrical Characteristics for MIPI CDPHY interface

Parameters	Symbol	Description	Test condition	Min	Typ	Max	Unit
LP-RX	V_{IH}	Logic1 input voltage	All conditions	880	NA	NA	mV

Parameters	Symbol	Description	Test condition	Min	Typ	Max	Unit
	V_{IL}	Logic0 input voltage, not in ULPS state	All conditions	NA	NA	550	mV
Skew Calibration	$T_{skewcal}$ (initial)	Duration for which the transmitter drives the skew-calibration pattern in the initial skew calibration mode	>1.5Gbps	NA	NA	100	us
				2^15	NA	NA	UI
	$T_{skewcal}$ (periodic)	Duration for which the transmitter drives the skew-calibration pattern in the periodic skew calibration mode	>1.5Gbps (optional)	NA	NA	10	us
				2^13	NA	NA	UI

3.8 Electrical Characteristics for MIPI CSI DPHY interface

Table 3-10 Electrical Characteristics for MIPI CSI DPHY interface

Parameters	Symbol	Min	Typ	Max	Units
Common-mode interference beyond 450 MHz	ΔVCMRX(HF)	NA	NA	100	mV
		NA	NA	50	mV
Common-mode interference 50MHz-450MHz	ΔVCMRX(LF)	-50	NA	50	mV
		-25	NA	25	mV
Common-mode termination	CCM	NA	NA	60	pF
Input pulse rejection	eSPIKE	NA	NA	300	V.ps
Minimum pulse width response	TMIN-RX	20	NA	NA	ns
Peak interference amplitude	VINT	NA	NA	200	mV
Interference frequency	fINT	450	NA	NA	MHz

3.9 Electrical Characteristics for SARADC

Table 3-11 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution			NA	12	NA	Bit
Anglog Input Range	AIN		AVSS18	NA	AVDD18	V
Differential Non-Linearity	DNL	PD = Low F_s = 1MS/s F_{CLK} = 20MHz F_{SOC} = 1MHz F_{AIN} = 10kHz ramp wave	NA	±1.0	±3.0	LSB
Integral Non-Linearity	INL		NA	±2.0	±6.0	LSB
Top Offset Voltage Error	E_{OT}		NA	±10	±20	LSB
Bottom Offset Voltage Error	E_{OB}		NA	±10	±20	LSB

3.10 Electrical Characteristics for TSADC

Table 3-12 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Accuracy from -40℃ to 125℃	T_{JACC}	Temp: -40 ~ 125℃ Supply: 1.62V ~ 1.98V	NA	±3	±5	℃
Sensing Temperature Range	T_{RANGE}		-40	NA	125	℃
Resolution	T_{LSB}		NA	1	NA	℃

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit	Note
Junction-to-ambient thermal resistance	$\boldsymbol{\theta_{JA}}$	15.84	$(℃/\boldsymbol{W})$	(1)
Junction-to-board thermal resistance	$\boldsymbol{\theta_{JB}}$	6.96	$(℃/\boldsymbol{W})$	(2)
Junction-to-case thermal resistance	$\boldsymbol{\theta_{JC}}$	0.67	$(℃/\boldsymbol{W})$	(3)
Thermal characterization parameter	$\boldsymbol{\psi_{JT}}$	0.031	$(℃/\boldsymbol{W})$	(4)

Note (1): The package-board system is placed in the natural convection (JEDEC JESD51-2 standard), and the 2S2P test-board is designed in accordance with JESD 51-7/JESD 51-9. The actual system design and environment may be different.

Note (2): $\boldsymbol{\theta_{JB}}$ is measured in the special environment (JEDEC JESD51-8 standard), and the printed circuit board used to mount the devices is specified in JESD51-7.

Note (3): The thermal resistance $\boldsymbol{\theta_{JC}}$ is provided in compliance with the JEDEC JESD51-14.

Note (4): The thermal characterization parameter $\boldsymbol{\psi_{JT}}$ is to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package, $\boldsymbol{\psi_{JT}}$ is measured in the test environment of $\boldsymbol{\theta_{JA}}$ (JEDEC JESD51-2 standard).